SI-842-6
File D04A

Standard Factory-Stored Programs

for the INTERSHAKE System

OCTOBER 1979

ATLANTIC RESEARCH CORPORATION
TELEPRODUCT®
ALEXANDRIA, VIRGINIA 22314

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File D04A

Standard Factory-Stored Programs

for the INTERSHAKE System

ATLANTIC RESEARCH CORPORATION
TELEPRODUCTS DIVISION
5390 Cherokee Avenue, Alexandria, Virginia 22314

OCTOBER 1979

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Foreword

INTERSHAKE PROM File D04A contains a new set of programs that supercede File D04 and its associated documentation. The present manual applies to the Factory-Stored Programs of File D04A, comprising PROMS 842E-004C, 842F-004C, and 842G-001B.

Atlantic Research Corporation reserves the right to further revise this firmware.

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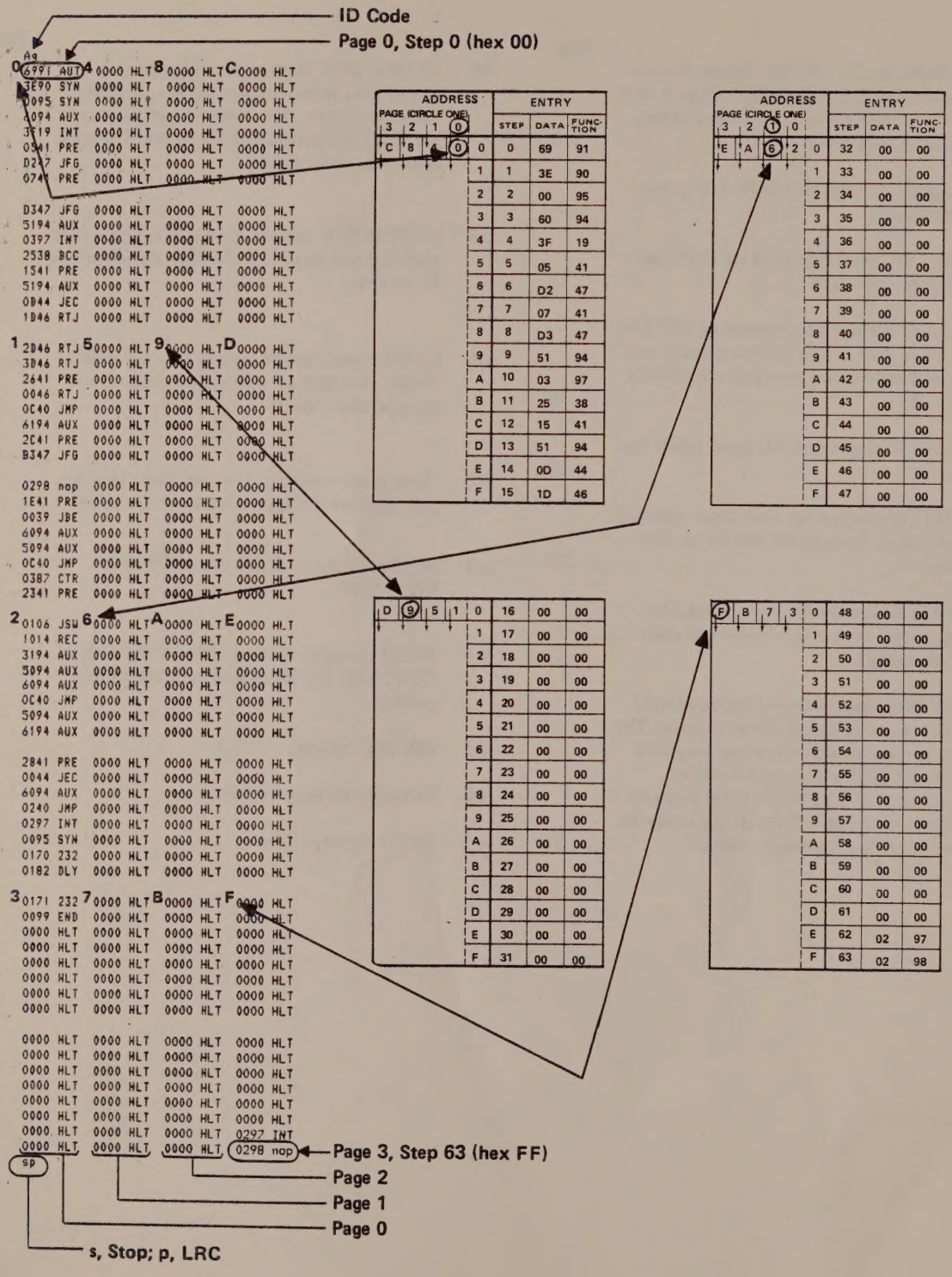

ID Code
Page 0, Step 0 (hex 00)
Page 3, Step 63 (hex FF)
Page 2
Page 1
Page 0
s, Stop; p, LRC
ADDRESS
PAGE (CIRCLE ONE)
3 2 1 0
ENTRY
STEP DATA FUNC-TION
C 8 4 0
E A 6 2
D 9 5 1
F B 7 3

1 Introduction

1.1 Overview

The INTERSHAKE firmware of File D04 consists of three PROMS. The programs are on the E (Data, or operand) PROM and the F (Function, or operation code) PROM. The G PROM stores the test messages called in the programs.

Four programs are supplied in File D04A: In PROM cell A-B is a Multi-Mode Monitor, a basic universal monitor program that allows menu selection of ASCII, EBCDIC, or SDLC, and SYNC or ASYNC monitoring. A CRC Loopback Test, Cell C-D, allows the user to perform a local or remote (where applicable) loopback on a communication circuit. Cell E-F incorporates a basic Self Test which should give the user a fair degree of assurance that the DTM-2 is functional. Cell G-H contains the 3270-3275 EBCDIC interactive test program from File D01.

These programs apply to the standard INTERSHAKE of Series F and above. They may require editing for modified equipment such as option M550. The program changes needed are not extensive and are explained thoroughly on an individual basis in the text.

This document covers the first three programs (Cells A-F) in File D04A. The EBCDIC 3270 program, Cell G-H, is covered by Document SI-842-2B, Protocol and Diagnostic Testing of 3270 Series Terminals, which is included in this binding. To run the EBCDIC 3270 program, the user should supplement File D04A with message PROM 842G-002B.

1.2 Loading Firmware Stored Programs

All four programs are 256 steps in length; therefore, the DTM-2 internal DIP switch 5 must be in the ON position. The INTERSHAKE front panel controls are shown in Appendix B.

1. Depress the LOAD button in zone 4.
2. Select the program to be executed by setting the LOAD STORED TEST switch (zone 8) to the PROM cell location of the desired test.
3. Depress the STEP button (zone 7).
4. Move the toggle switch (manual-single step-auto) in zone 8 to the AUTO position.
5. Depress the ENTER button (zone 8).

The selected program is now in the appropriate RAM cell ready for execution. The first instruction of the selected program should appear in the DTM-2 processor display window (zone 7).

6. Return the MANUAL-SINGLE STEP-AUTO switch to the MANUAL position.

1.3 Running the Program

1. Select the appropriate RAM cell using the LOAD STORED TEST switch. NOTE: In the standard INTERSHAKE, firmware stored tests will automatically be loaded into RAM cell A (or A-B). In the M550 modification, the contents of the PROM cells load in parallel into the corresponding RAM cells; i.e., when PROM cell C-D is selected, it loads into RAM cell C-D.
2. In zone 8 of the INTERSHAKE face panel are eight numbered toggle switches, called bit switches or sense switches. These should all be in the SPACE (off) position when the setup for a program in begun.
3. Follow any special setup instructions for the test that has been loaded.
4. Depress the RUN or KYBD button (zone 4).

The program may now be started via any of the methods available with the INTERSHAKE system.

1.4 Reading an Inter-KEY Program Listing

This section is provided to aid the user in understanding the Inter-KEY listings and DTM-2 programs. It should be of special value in employing the Inter-KEY editor modes.

The address and entry columns to the right of the Inter-KEY program listing on the opposite page are adapted from the INTERSHAKE II Program Sheet to show the correspondence between the listing and the program sheet.

One side of an INTERSHAKE program sheet contains a total of 32 steps; thus 64 steps fit on one sheet (both sides); and four full program sheets are required for a full 256-step program.

The program sheet carries both hexadecimal and decimal step-page addresses.

Program steps are usually identified by the two-digit hexadecimal addresses, from 00 to FF. In the editor mode the INTERSHAKE program is displayed on the CRT in its hexadecimal address form, and hexadecimal addresses must be used in writing cross-referenced instructions within programs.

In the INTERSHAKE panel display (Zone 7), program addresses are shown in decimal form: Steps 0-63, Pages 0-3.

One column of the Inter-KEY listing represents one program memory page and corresponds to one full program sheet; four columns, to four full program sheets or one full-cell 256-step program.

The columns are divided into groups of eight instructions to make it easier to locate specific addresses.

The three-character mnemonics facilitate recognition of the corresponding functions.

The term *data* is synonymous with operand; *function* is used for operation code. INTERSHAKE instructions are always written in the order data-function.

2 Multi-Mode Monitor (Cell A-B)

2.1 Description

This program allows the user to monitor data under prescribed conditions. However, in some system modes, such as true FDX, data may be incorrectly displayed unless the test is modified. The program can be edited easily for any application.

Figure 2-1 is a listing of the program as it appears in the INTERSHAKE LOAD mode display.

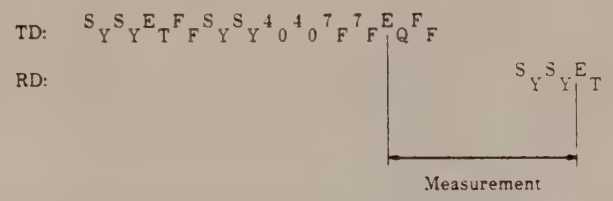
The user may select any of five applications from menu instructions that are displayed when the basic program is being executed (see Figure 2-2). These options use extensive auto-panel functions. Only three manual steps need be performed.

1. Asynchronous speed (bit rate, zone 1) must be selected.
2. The MON SIGS OUT switch (zone 3) must be in NORMAL position.
3. One of the following five monitors may be selected by turning on the designated bit switch and pressing the STEP button.

Monitors 1 and 2 Synchronous monitors 1 and 2 assume respectively odd and even parity ASCII HDX BISYNC applications.

Monitor 3 Number 3 selects EBCDIC (3270 type) with auto synchronization enabled.

This version also includes a visual response-time measurement, which is only effective for 3270 protocol and measures the time from the ENQ character to the first non-sync character received. For example,



The response measurement requires manual setting of the counter input switch to DURATION and of the range switch to the appropriate range, probably 10^2-10^3.

Monitor 4 Number 4 selects an SDLC-NRZ monitor. Because SDLC is predominantly FDX, the program auto-panels to TD lead only. The INTERVIEW may be placed in the FDX position to monitor both TD and RD, and the BB93 instruction at location 20_{16} edited to reverse lead selection. HDX TD or RD may be chosen when necessary.

The program may be modified for SDLC-NRZI simply by editing Instruction 1096 at location $1E_{16}$ to 3096.

Monitor 5 Asynchronous ASCII, even or odd parity, is assumed. The operator must match the DTM-2 internal bit rate to that of the system being monitored. This monitor will automatically select the correct parity for the link being monitored.

For automatic parity error counting, set the counter input switch to PE 10^X. Parity errors will be displayed in half-intensity video on the INTERVIEW.

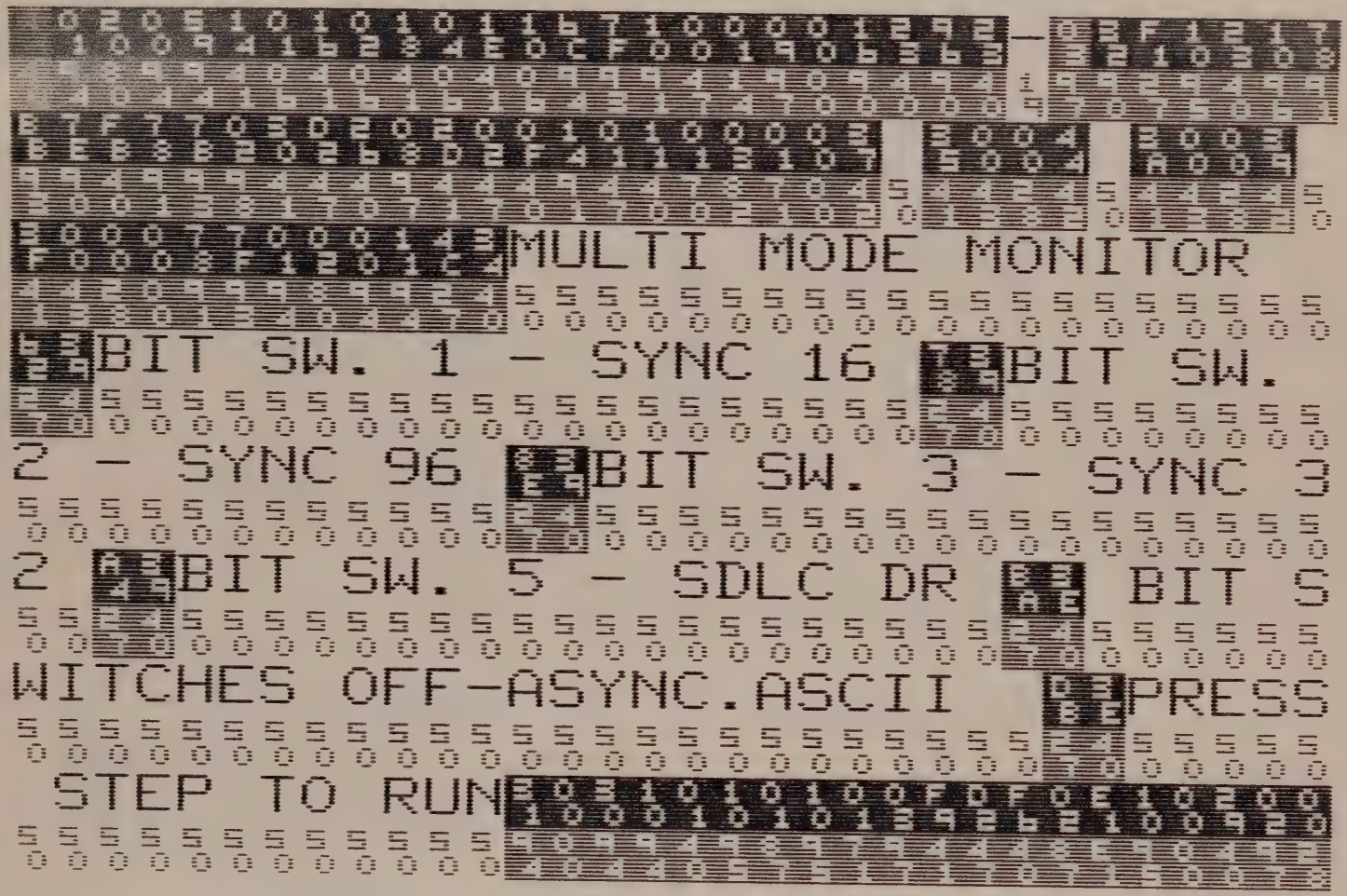


FIGURE 2-1 LOAD mode display of Multi-Mode Monitor program on INTERVIEW CRT, Page 1 or 2. (Note: This display will not be seen unless the operator specifies it.)

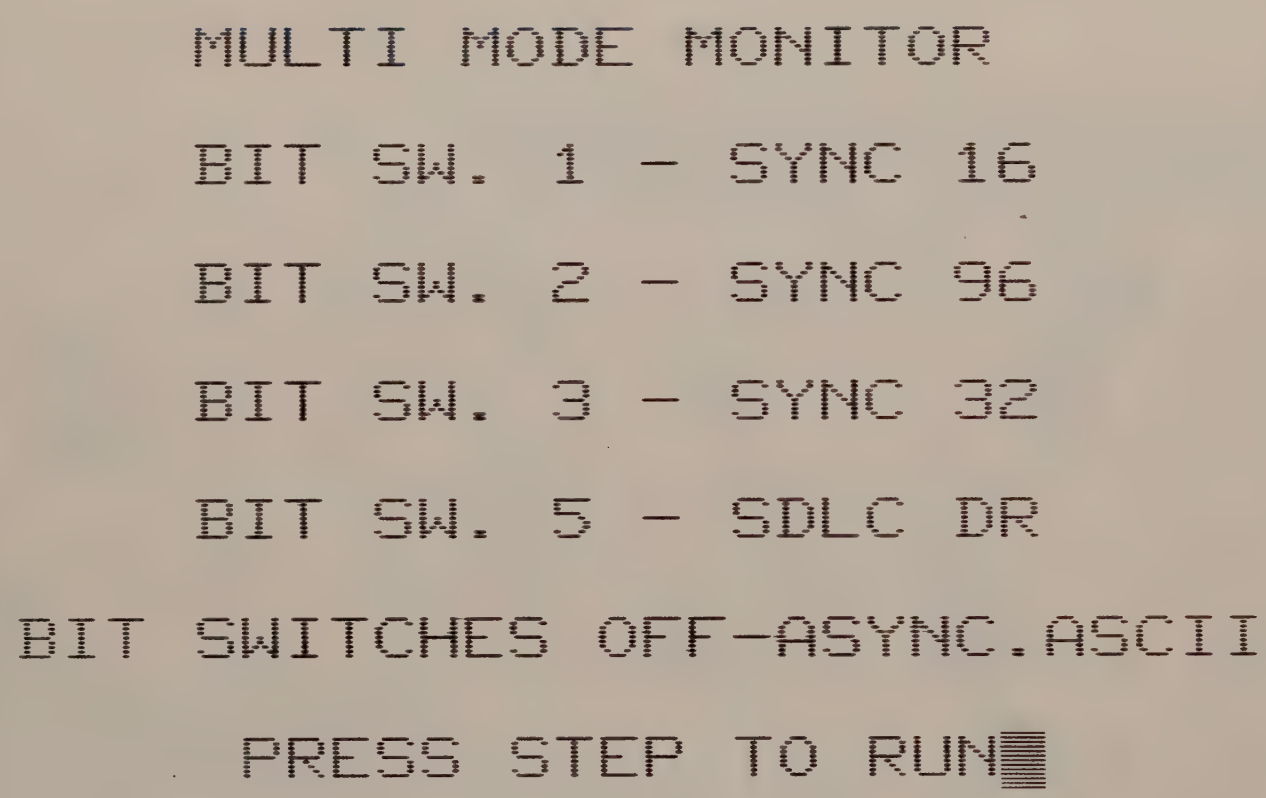
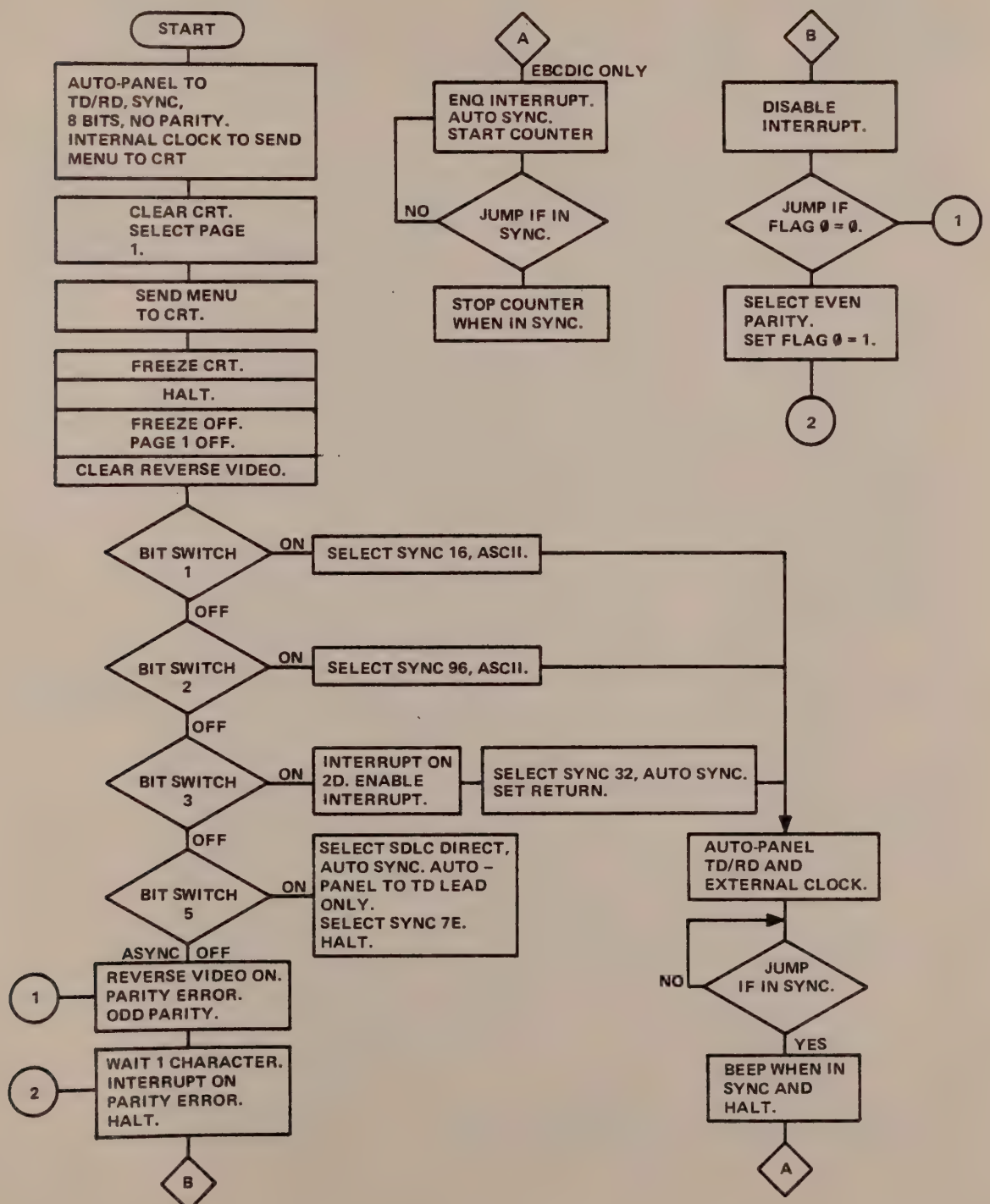

MULTI MODE MONITOR
BIT SW. 1 - SYNC 16
BIT SW. 2 - SYNC 96
BIT SW. 3 - SYNC 32
BIT SW. 5 - SDLC DR
BIT SWITCHES OFF-ASYNC.ASCI
PRESS STEP TO RUN

FIGURE 2-2 CRT display of menu selection during program execution.

2.2 Program Flow Diagram



2.3 Program

INTERSHAKE II PROGRAM

TITLE: MULTI-MODE MONITOR

FILE NO. D04A
SHEET 1 OF 4

DESCRIPTION:
Auto-panel functions are used extensively. DTM-2 front panel setup does not apply, other than counter switches for 3270 EBCDIC monitoring.

PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 4 (0)	0	0	44	40	Go-to.	
	1	1	01	94	Clear CRT.	
	2	2	20	80		
	3	3	00	94		
	4	4	59	94	Reverse video on all receive data.	
	5	5	14	41	Load address register.	
	6	6	01	06	Jump if bit switches = 01_{16}.	
	7	7	16	41	Load address register.	
	8	8	02	06	Jump if bit switches = 02_{16}.	
	9	9	18	41	Load address register.	
	A	10	04	06	Jump if bit switches = 04_{16}.	
	B	11	1E	41	Load address register.	
	C	12	10	06	Jump if bit switches = 10_{16}.	
	D	13	6C	94	Half-intensity on parity error.	
	E	14	7F	93	Auto-panel.	
	F	15	10	91	Auto-panel.	
D 9 5 (1)	0	16	00	47	Set Flag 0 = 0.	
	1	17	01	14	Wait 1 character.	
	2	18	09	97	Interrupt on parity error.	
	3	19	00	00	Halt.	
	4	20	16	90	Load 16_{16} sync character.	
	5	21	23	40	Go-to.	
	6	22	96	90	Load 96_{16} sync character.	
	7	23	23	40	Go-to.	
	8	24	2D	19	Load interrupt character.	
	9	25	03	97	Enable interrupt.	
	A	26	32	90	Load 32_{16} sync character.	
	B	27	F1	27	Set return address.	
	C	28	10	95	Auto-sync enabled.	
	D	29	23	40	Go-to.	
	E	30	10	96	SDLC 0 insert mode on.	
	F	31	78	91	8 Bits, no parity, sync mode.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE
SPEED
ASYNC / SYNC
SYN CHARACTER
STOP BIT 1.0 , 1.5 , 2.0
INFO BITS 5 , 6 , 7 , 8
PARITY NONE , ODD , EVEN
CONTROL EIA / OFF
ON-LINE TD/RD , TD , RD
OFF-LINE TERM / MODEM
MON SIGS / NORMAL
PATCH CORDS
CONTROL EIA (V.24)
COUNTER ZONE
DURATION
10^0 - 10^8
Length
INTERRUPTS
FLAGS
LATCH

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A 6 2	0	32	BB	93	Auto-panel to TD, ext. clock, EIA	
	1	33	7E	90	Load $7E_{16}$ frame sync character.	
	2	34	FB	40	Go-to.	
	3	35	78	91	Auto-panel: 8 bit, no parity, sync.	
	4	36	7B	93	Auto-panel: TD/RD, ext. clock, EIA.	
	5	37	02	98	No-op.	
	6	38	30	41	Load address register.	
	7	39	D2	47	Jump if in sync.	
	8	40	26	40	Go-to (if out of sync).	
	9	41	08	97	Disable interrupt.	
	A	42	2D	41	Load address register.	
	B	43	02	47	Jump if Flag 0 = 0.	
	C	44	0F	40	Go-to.	
	D	45	14	91	Auto-panel.	
	E	46	01	47	Set Flag 0 = 1.	
	F	47	11	40	Go-to.	
F B 7 3	0	48	01	70	Alarm on.	
	1	49	03	82	Wait 300 ms.	
	2	50	01	71	Alarm off.	
	3	51	00	00	Halt.	
	4	52	37	42	} Send 37 spaces.	
	5	53	A0	50		
	6	54	35	41		
	7	55	00	43		
	8	56	00	28	Return.	
	9	57	44	42	} Send 44 spaces.	
	A	58	A0	50		
	B	59	3A	41		
	C	60	00	43		
	D	61	00	28	Return.	
	E	62	39	42	} Send 39 spaces.	
	F	63	A0	50		

FILE NO. D04A
SHEET 15 OF 4
PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 2 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 (4) 0	0	0	3F	41		
	1	1	00	43		
	2	2	00	28	Return.	
	3	3	00	00		
	4	4	78	91	Auto-panel for menu.	
	5	5	7F	93	Auto-panel.	
	6	6	01	94		
	7	7	02	80	Clear CRT.	
	8	8	00	94		
	9	9	11	94	Select Page 1 on CRT.	
	A	10	4C	27	Set address.	
	B	11	34	40	Go-to.	
	C	12	4D	50	Send M.	
	D	13	55	50	Send U.	
	E	14	CC	50	Send L.	
	F	15	D4	50	Send T.	
D 9 (5) 1	0	16	C9	50	Send I.	
	1	17	A0	50	Send space.	
	2	18	4D	50	Send M.	
	3	19	CF	50	Send O.	
	4	20	44	50	Send D.	
	5	21	C5	50	Send E.	
	6	22	A0	50	Send space.	
	7	23	4D	50	Send M.	
	8	24	CF	50	Send O.	
	9	25	4E	50	Send N.	
	A	26	C9	50	Send I.	
	B	27	D4	50	Send T.	
	C	28	CF	50	Send O.	
	D	29	D2	50	Send R.	
	E	30	A0	50	Send space.	
	F	31	A0	50	Send space.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE
SPEED
ASYNC / SYNC
SYN CHARACTER
STOP BIT 1.0 , 1.5 , 2.0
INFO BITS 5 , 6 , 7 , 8
PARITY NONE , ODD , EVEN
CONTROL EIA / OFF
ON-LINE TD/RD , TD , RD
OFF-LINE TERM / MODEM
MON SIGS / NORMAL
PATCH CORDS
CONTROL EIA (V. 24)
COUNTER ZONE
INTERRUPTS
FLAGS
LATCH

CONTINUE ON OTHER SIDE

CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A (6) 2	0	32	62	27	Set address.	
	1	33	39	40	Go-to (get spaces).	
	2	34	42	50	Send B.	
	3	35	C9	50	Send I.	
	4	36	D4	50	Send T.	
	5	37	A0	50	Send space.	
	6	38	53	50	Send S.	
	7	39	D7	50	Send W.	
	8	40	2E	50	Send period.	
	9	41	A0	50	Send space.	
	A	42	B1	50	Send 1.	
	B	43	A0	50	Send space.	
	C	44	2D	50	Send -.	
	D	45	A0	50	Send space.	
	E	46	53	50	Send S.	
	F	47	59	50	Send Y.	
F B (7) 3	0	48	4E	50	Send N.	
	1	49	C3	50	Send C.	
	2	50	A0	50	Send space.	
	3	51	B1	50	Send 1.	
	4	52	36	50	Send 6.	
	5	53	A0	50	Send space.	
	6	54	78	27	Set address.	
	7	55	39	40	Go-to (get spaces).	
	8	56	42	50	Send B.	
	9	57	C9	50	Send I.	
	A	58	D4	50	Send T.	
	B	59	A0	50	Send space.	
	C	60	53	50	Send S.	
	D	61	D7	50	Send W.	
	E	62	2E	50	Send period.	
	F	63	A0	50	Send space.	

FILE NO. D04A
SHEET 2 OF 4
PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

DESCRIPTION:

OBJECTIVE:

FILE NO. D04A
SHEET 3 OF 4
PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM

ADDRESS PAGE (CIRCLE ONE) 3 (2) 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C (8) 4 0	0	0	B2	50	Send 2.	
	1	1	A0	50	Send space.	
	2	2	2D	50	Send -.	
	3	3	A0	50	Send space.	
	4	4	53	50	Send S.	
	5	5	59	50	Send Y.	
	6	6	4E	50	Send N.	
	7	7	C3	50	Send C.	
	8	8	A0	50	Send space.	
	9	9	39	50	Send 9.	
	A	10	36	50	Send 6.	
	B	11	A0	50	Send space.	
	C	12	8E	27	Set address.	
	D	13	39	40	Go-to.	
	E	14	42	50	Send B.	
	F	15	C9	50	Send I.	
D (9) 5 1	0	16	D4	50	Send T.	
	1	17	A0	50	Send space.	
	2	18	53	50	Send S.	
	3	19	D7	50	Send W.	
	4	20	2E	50	Send period.	
	5	21	A0	50	Send space.	
	6	22	33	50	Send 3.	
	7	23	A0	50	Send space.	
	8	24	2D	50	Send -.	
	9	25	A0	50	Send space.	
	A	26	53	50	Send S.	
	B	27	59	50	Send Y.	
	C	28	4E	50	Send N.	
	D	29	C3	50	Send C.	
	E	30	A0	50	Send space.	
	F	31	33	50	Send 3.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE

SPEED

ASYNC / SYNC

SYN CHARACTER

STOP BIT 1.0 , 1.5 , 2.0

INFO BITS 5 , 6 , 7 , 8

PARITY NONE , ODD , EVEN

CONTROL EIA / OFF

ON-LINE TD/RD , TD , RD

OFF-LINE TERM / MODEM

MON SIGS / NORMAL

PATCH CORDS

CONTROL EIA (V.24)

COUNTER ZONE

INTERRUPTS

FLAGS

LATCH

CONTINUE ON OTHER SIDE

CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
(E) A 6 2	0	32	A0	50	Send space.	
	1	33	53	50	Send S.	
	2	34	D4	50	Send T.	
	3	35	C5	50	Send E.	
	4	36	50	50	Send P.	
	5	37	A0	50	Send space.	
	6	38	D4	50	Send T.	
	7	39	CF	50	Send O.	
	8	40	A0	50	Send space.	
	9	41	D2	50	Send R.	
	A	42	55	50	Send U.	
	B	43	4E	50	Send N.	
	C	44	31	94	Freeze CRT.	
	D	45	00	00	Halt (wait for step button).	
	E	46	30	94	Unfreeze CRT.	
	F	47	10	94	Page 1 off.	
(F) B 7 3	0	48	01	40	Go-to.	
	1	49	10	95	Auto sync on.	
	2	50	01	87	Start counter.	
	3	51	10	95	Auto sync on (force 00).	
	4	52	01	71	Alarm off.	
	5	53	03	97	Enable character interrupt.	
	6	54	F9	41	Load address register.	
	7	55	D2	47	Jump if in sync.	
	8	56	F6	40	Go-to.	
	9	57	02	87	Stop counter.	
	A	58	E1	E1	EOF.	
	B	59	10	95	Auto sync on.	
	C	60	00	00	Halt.	
	D	61	29	40	Go-to.	
	E	62	02	97	Disable character interrupt.	
	F	63	00	28	Return.	

FILE NO. D04A
SHEET 4B OF 4
PROGRAM LOCATION
DTM S/N
CELL A-B
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: John A. Mansker DATE

COMPANY NAME: Atlantic Research Corporation TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

2.4 Inter-KEY Program Listing

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Ag
4440 JMP  3F41 PRE  B250 XMT  D750 XMT
0194 AUX  0043 JEL  A050 XMT  C950 XMT
2080 DLY  0028 RET  2D50 XMT  D450 XMT
0094 AUX  0000 HLT  A050 XMT  C350 XMT
5994 AUX  7891 AUT  5350 XMT  4850 XMT
1441 PRE  7F93 AUT  5950 XMT  C550 XMT
0106 JSW  0194 AUX  4E50 XMT  5350 XMT
1641 PRE  0280 DLY  C350 XMT  A050 XMT

0206 JSW  0094 AUX  A050 XMT  CF50 XMT
1841 PRE  1194 AUX  3950 XMT  C650 XMT
0406 JSW  4C27 PRE  3650 XMT  C650 XMT
1E41 PRE  3440 JMP  A050 XMT  2D50 XMT
1006 JSW  4D50 XMT  8E27 PRE  4150 XMT
6C94 AUX  5550 XMT  3940 JMP  5350 XMT
7F93 AUT  CC50 XMT  4250 XMT  5950 XMT
1091 AUT  D450 XMT  C950 XMT  4E50 XMT

0047 FLG  C950 XMT  D450 XMT  C350 XMT
0114 REC  A050 XMT  A050 XMT  2E50 XMT
0997 INT  4D50 XMT  5350 XMT  4150 XMT
0000 HLT  CF50 XMT  D750 XMT  5350 XMT
1690 SYN  4450 XMT  2E50 XMT  C350 XMT
2340 JMP  C550 XMT  A050 XMT  C950 XMT
9690 SYN  A050 XMT  3350 XMT  C950 XMT
2340 JMP  4D50 XMT  A050 XMT  A050 XMT

2D19 INT  CF50 XMT  2D50 XMT  A050 XMT
0397 INT  4E50 XMT  A050 XMT  DB27 PRE
3290 SYN  C950 XMT  5350 XMT  3E40 JMP
F127 PRE  D450 XMT  5950 XMT  5050 XMT
1095 SYN  CF50 XMT  4E50 XMT  D250 XMT
2340 JMP  D250 XMT  C350 XMT  C550 XMT
1096 AUT  A050 XMT  A050 XMT  5350 XMT
7891 AUT  A050 XMT  3350 XMT  5350 XMT

BB93 AUT  6227 PRE  B250 XMT  A050 XMT
7E90 SYN  3940 JMP  A050 XMT  5350 XMT
FB40 JMP  4250 XMT  A427 PRE  D450 XMT
7891 AUT  C950 XMT  3940 JMP  C550 XMT
7B93 AUT  D450 XMT  4250 XMT  5050 XMT
0298 nop  A050 XMT  C950 XMT  A050 XMT
3041 PRE  5350 XMT  D450 XMT  D450 XMT
D247 JFG  D750 XMT  A050 XMT  CF50 XMT

2640 JMP  2E50 XMT  5350 XMT  A050 XMT
0897 INT  A050 XMT  D750 XMT  D250 XMT
2D41 PRE  B150 XMT  2E50 XMT  5550 XMT
0247 JFG  A050 XMT  A050 XMT  4E50 XMT
0F40 JMP  2D50 XMT  3550 XMT  3194 AUX
1491 AUT  A050 XMT  A050 XMT  0000 HLT
0147 FLG  5350 XMT  2D50 XMT  3094 AUX
1140 JMP  5950 XMT  A050 XMT  1094 AUX

0170 232  4E50 XMT  5350 XMT  0140 JMP
0382 DLY  C350 XMT  4450 XMT  1095 SYN
0171 232  A050 XMT  CC50 XMT  0187 CTR
0000 HLT  B150 XMT  C350 XMT  1095 SYN
3742 PRE  3650 XMT  A050 XMT  0171 232
A050 XMT  A050 XMT  4450 XMT  0397 INT
3541 PRE  7827 PRE  D250 XMT  F941 PRE
0043 JEL  3940 JMP  A050 XMT  D247 JFG

0028 RET  4250 XMT  BA27 PRE  F640 JMP
4442 PRE  C950 XMT  3E40 JMP  0287 CTR
A050 XMT  D450 XMT  A050 XMT  E1E1 EOF
3A41 PRE  A050 XMT  4250 XMT  1095 SYN
0043 JEL  5350 XMT  C950 XMT  0000 HLT
0028 RET  D750 XMT  D450 XMT  2940 JMP
3942 PRE  2E50 XMT  A050 XMT  0297 INT
A050 XMT  A050 XMT  5350 XMT  0028 RET
sV
```

3 CRC Loopback Test (Cell C-D)

This test is useful on line as well as for demonstration purposes. It is designed to give the user a measurement of his communication link's reliability. The program allows him to look at the communication link in the same light that his computer system uses that link and to obtain an error rate per *N* data blocks.

When it is executed, the program displays a basic menu on the CRT, as shown in Figure 3-1. This serves as a reminder to the operator that certain control switches must be correctly set before the program will run properly. See Sections 3.7 and 3.8 for complete setup instructions.

The INTERVIEW LOAD mode display of the program is shown in Figure 3-2.

3.1 Description

The program tests the communication link in a loopback configuration, local digital or analog, remote analog or digital, or any loopback designed to accurately reproduce transmitted data at the receiving, or origination, point.

The operator may transmit 10 to 10^8 blocks of data at rates from 1200 bps to 62 kbps.

ASCII even parity and CRC-16 were selected to give the user the maximum ability to determine any faults on his communication link.

Transmitted blocks are displayed on the INTERVIEW in normal full-intensity video; received blocks, in reverse video (see Figure 3-3). Test blocks that are found to have bad CRC are followed with a blinking "BAD BCC" message (see Figure 3-4). Any parity errors occurring (odd parity) will be displayed in reverse half-intensity (see Figure 3-5).

The choice of even-parity ASCII and CRC allows the user to determine bit sensitivity on the communication link as well as CRC for overall block errors.

3.2 Modem Conditioning

INTERSHAKE is attached to the link to be tested via its modem connector.

Modem position (zone 3) should be selected, and the RTS and DTR RS-232 switches enabled under program control (down). When initialized, the program turns on RTS and DTR; then waits 300 ms (user variable) for the modem to become ready.

On some modems, use of CTS in local loopback is optional. Therefore, no attempt has been made to test CTS within the program.

The program turns RLSD on, a fundamental requirement of most loopback tests. If no receive carrier is detected within 300 ms of initialization, the program will beep 6 times and flash "RLSD OFF" on the INTERVIEW to alert the operator (see Figure 3-6). Each program initialization attempt (for example, see Figure 3-7) is counted as an error, which may be either operator or modem error. After a valid loopback has been established, simply restart the program to obtain a correct error count.

After proper modem condition has been established, the program enables the RLSD interrupt. From this point on, any glitch on the RLSD lead (carrier hits on receive side only) locks the associated data block in the INTERVIEW, and FF_{16} is loaded into results memory for each hit. Thus a correlation between error count and carrier dropouts may be obtained.

3.3 Transmit Data Block

An initial loop counter groups all transmitted blocks by fives for self-test purposes. At the start of each transmit block the base counter is checked for END indication. This signifies that 10 to 10^8 blocks have been sent. Should the END indicator be ON, the program jumps to the ending sequence, stopping on Function 99 with the green complete LED (zone 3) lighted.

3.4 Self Test

The operator may introduce CRC errors by turning on bit switch 1 (bit switches now read 01_{16}). This sets Flag 0 to 1 every 6th transmit block. An inverted CRC is then calculated for that block. Since the receive section of the program calculates only normal CRC, it must detect an inverted CRC as a BCC error. The operator will find the 6th and 12th blocks displayed on the INTERVIEW with BAD BCC messages, along with 16 error counts for 10^2 blocks transmitted (see Figure 3-4). For 10 blocks transmitted, the INTERVIEW will display the 6th block (bad BCC) and last good block (see Figure 3-8).

3.5 Receive Data Block

Receive data blocks will be displayed on the INTERVIEW in reverse full-intensity video. Programs using CRC checking depend on two basic characters for proper operation: Receipt of STX signifies start of CRC calculation; receipt of ETX, ETB, or ITB, end of CRC calculation. Of the latter, only ETX is used in this program.

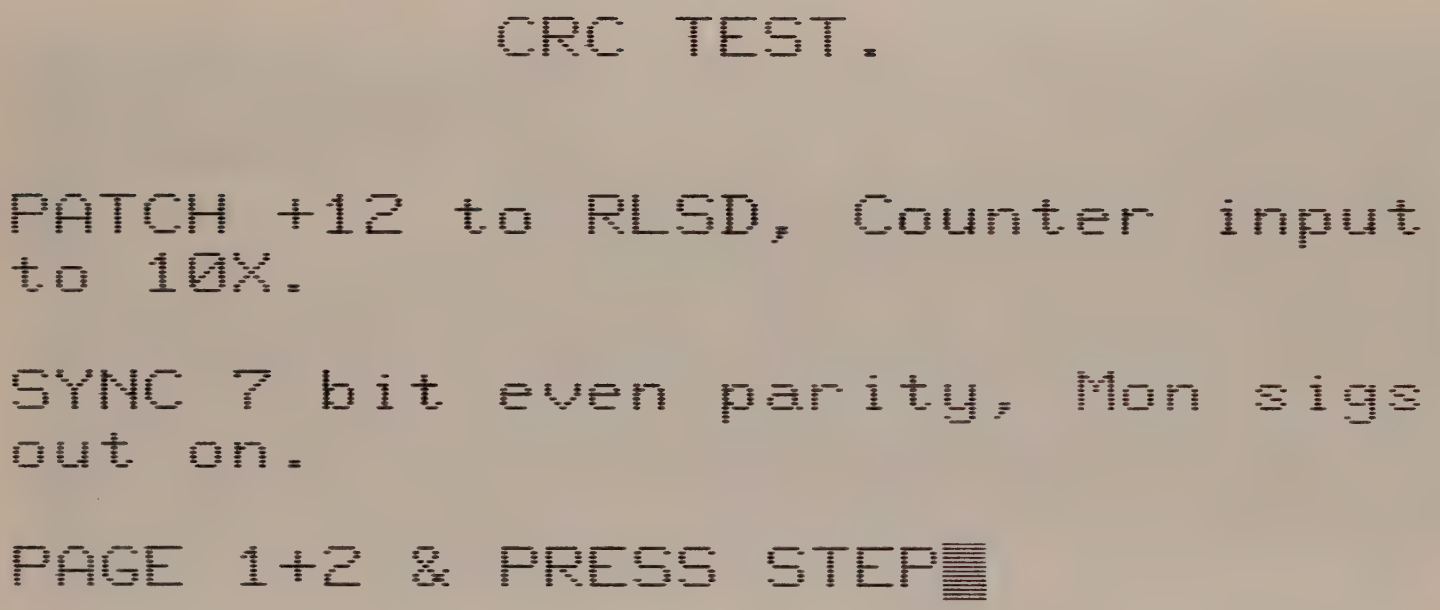


FIGURE 3-1 Menu for CRC test displayed on CRT during program execution.

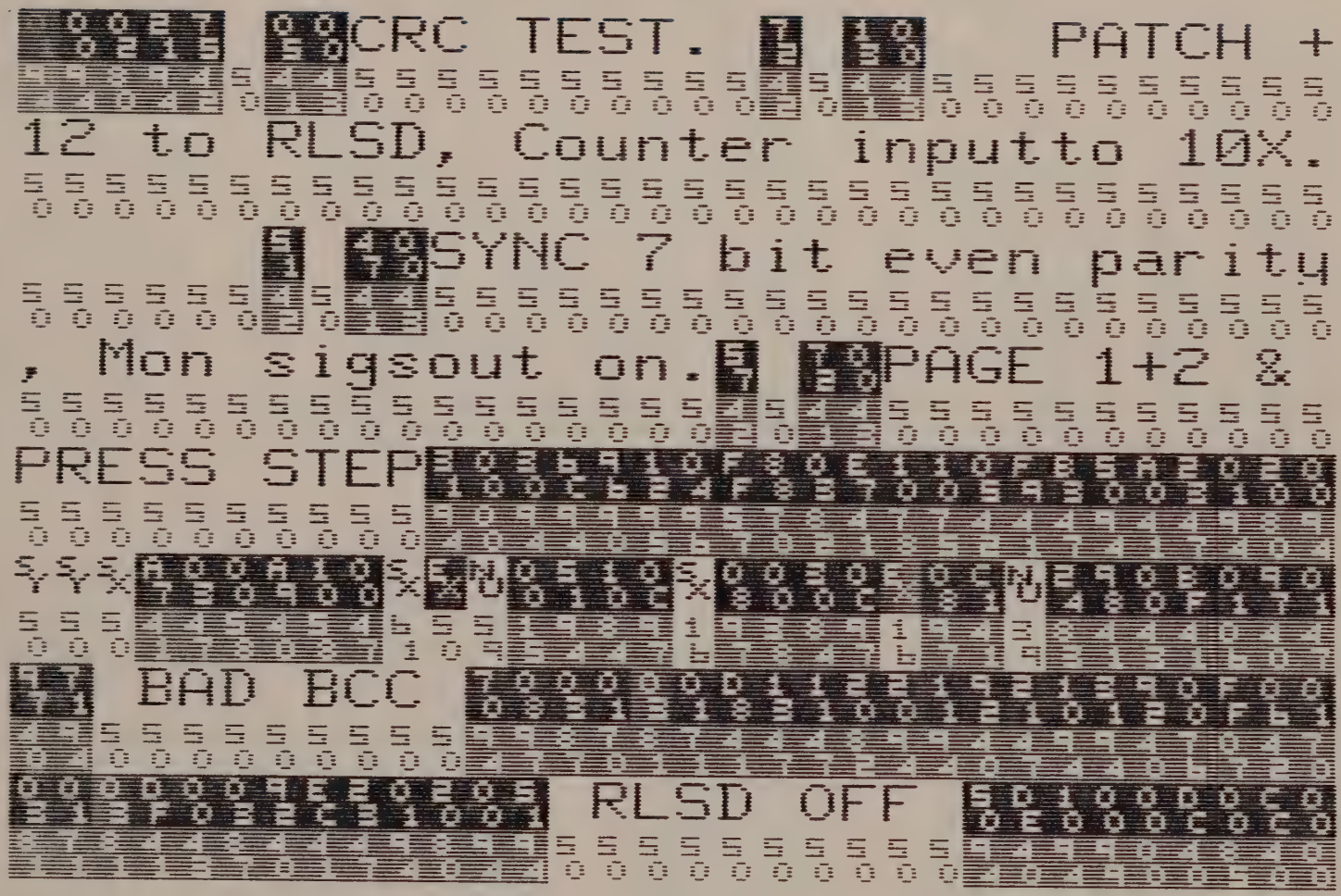


FIGURE 3-2 LOAD mode display of program on INTERVIEW, Page 1 or 2. (Note: This display will not be seen unless the operator specifically requests it.)

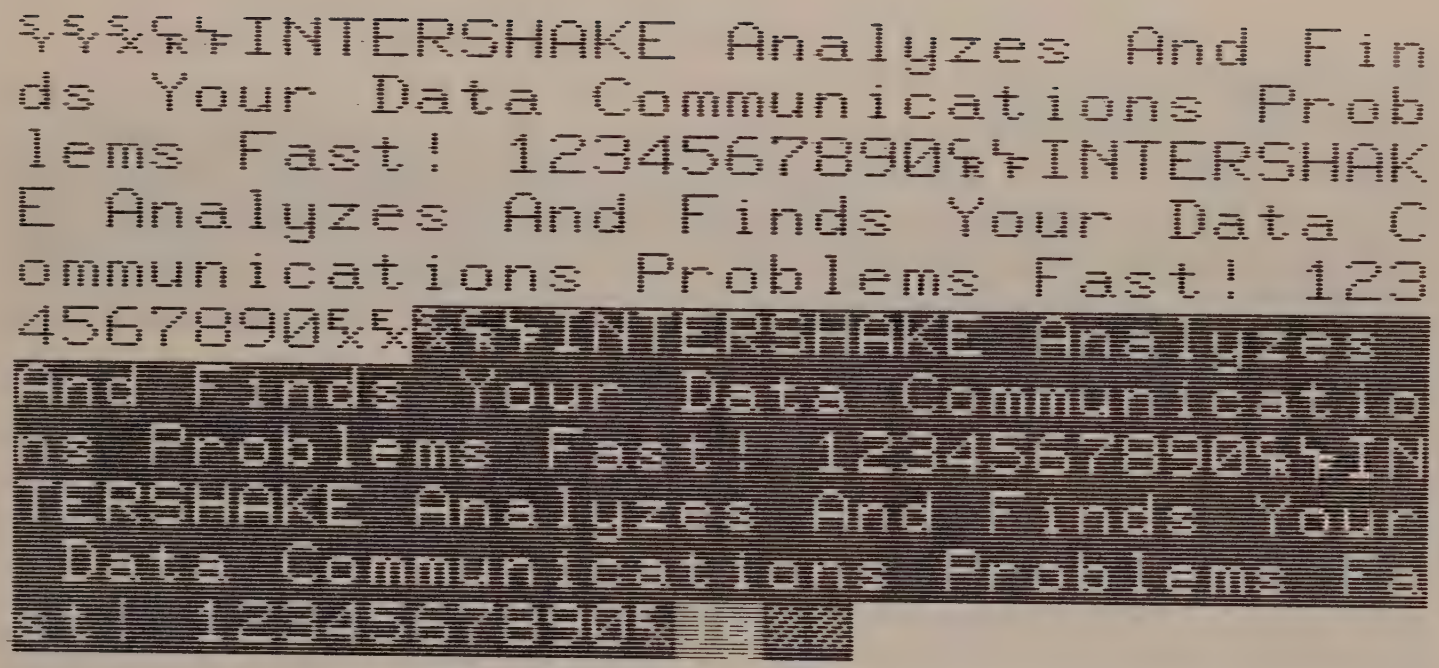

%%%&+INTERSHAKE Analyzes And Fin
ds Your Data Communications Prob
lems Fast! 1234567890&+INTERSHAK
E Analyzes And Finds Your Data C
ommunications Problems Fast! 123
4567890%%&&+INTERSHAKE Analyzes
And Finds Your Data Communicatio
ns Problems Fast! 1234567890&+IN
TERSHAKE Analyzes And Finds Your
Data Communications Problems Fa
st! 12345678905

FIGURE 3-3 INTERVIEW display of last good block (no errors).

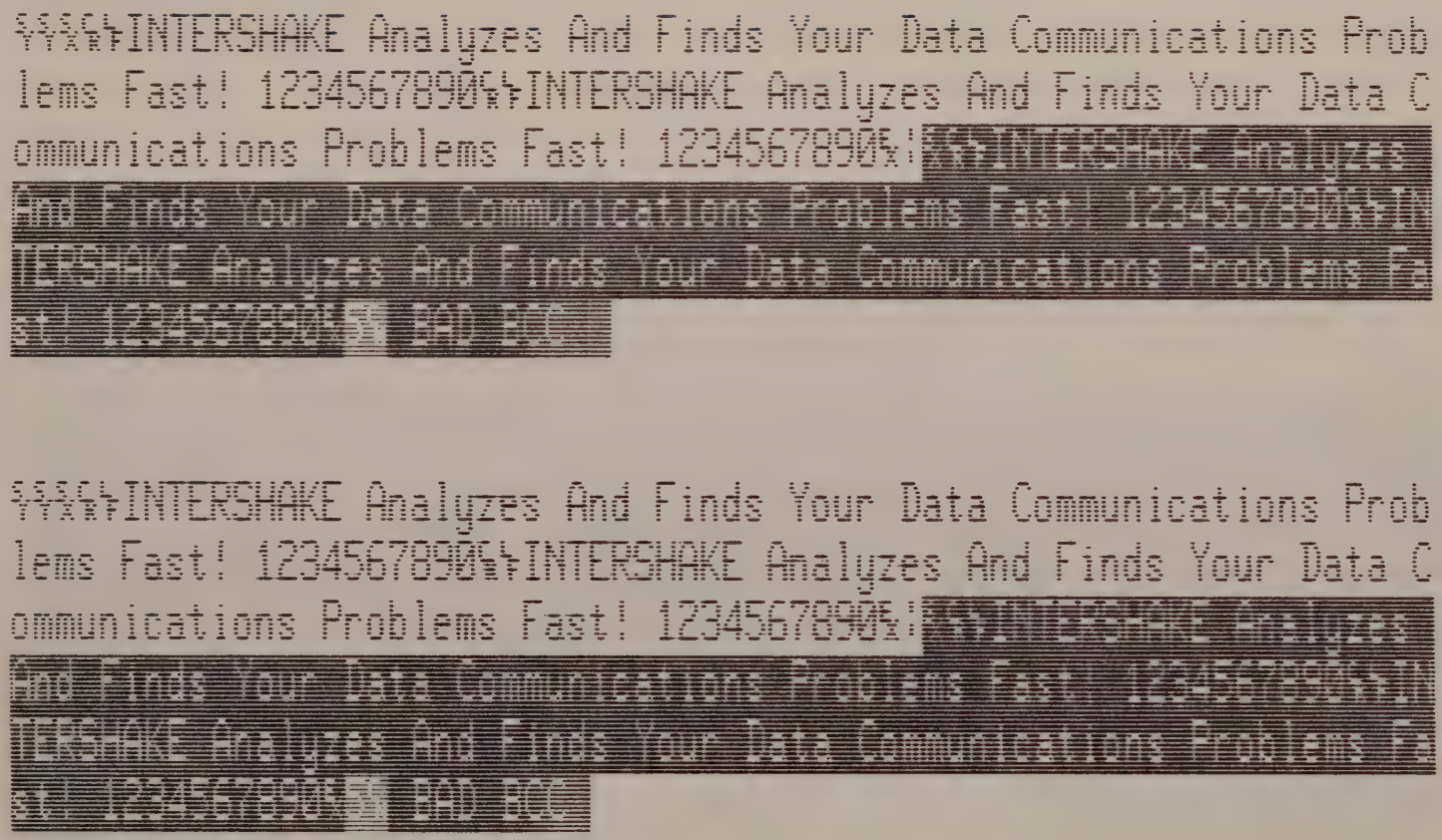

$%%%%INTERSHAKE Analyzes And Finds Your Data Communications Prob
lems Fast! 1234567890%%INTERSHAKE Analyzes And Finds Your Data C
ommunications Problems Fast! 1234567890%!
BAD BCC
$%%%%INTERSHAKE Analyzes And Finds Your Data Communications Prob
lems Fast! 1234567890%%INTERSHAKE Analyzes And Finds Your Data C
ommunications Problems Fast! 1234567890%!
BAD BCC

FIGURE 3-4 INTERVIEW display for Self Test, showing two bad blocks. Length switch set to 100 (10^2) blocks.

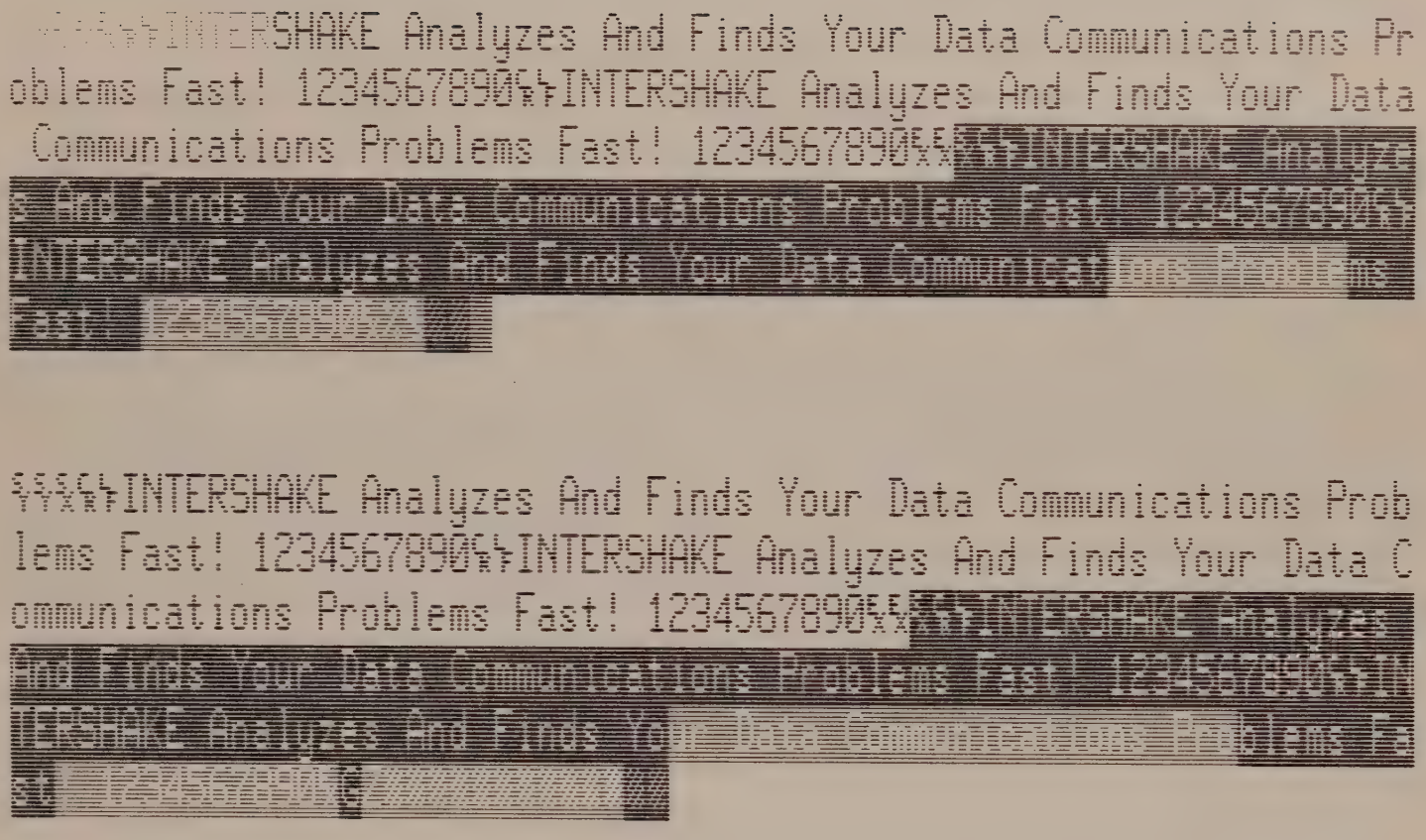

%%%%INTERSHAKE Analyzes And Finds Your Data Communications Problems Fast! 1234567890

FIGURE 3-6 INTERVIEW display on execution of program if there is no carrier from modem. The possible causes include (1) analog loopback not made; (2) RTS not on or defective; (3) bad modem; (4) INTERSHAKE plugged into wrong connector; (5) patch not made (in the case of off-line demonstration).

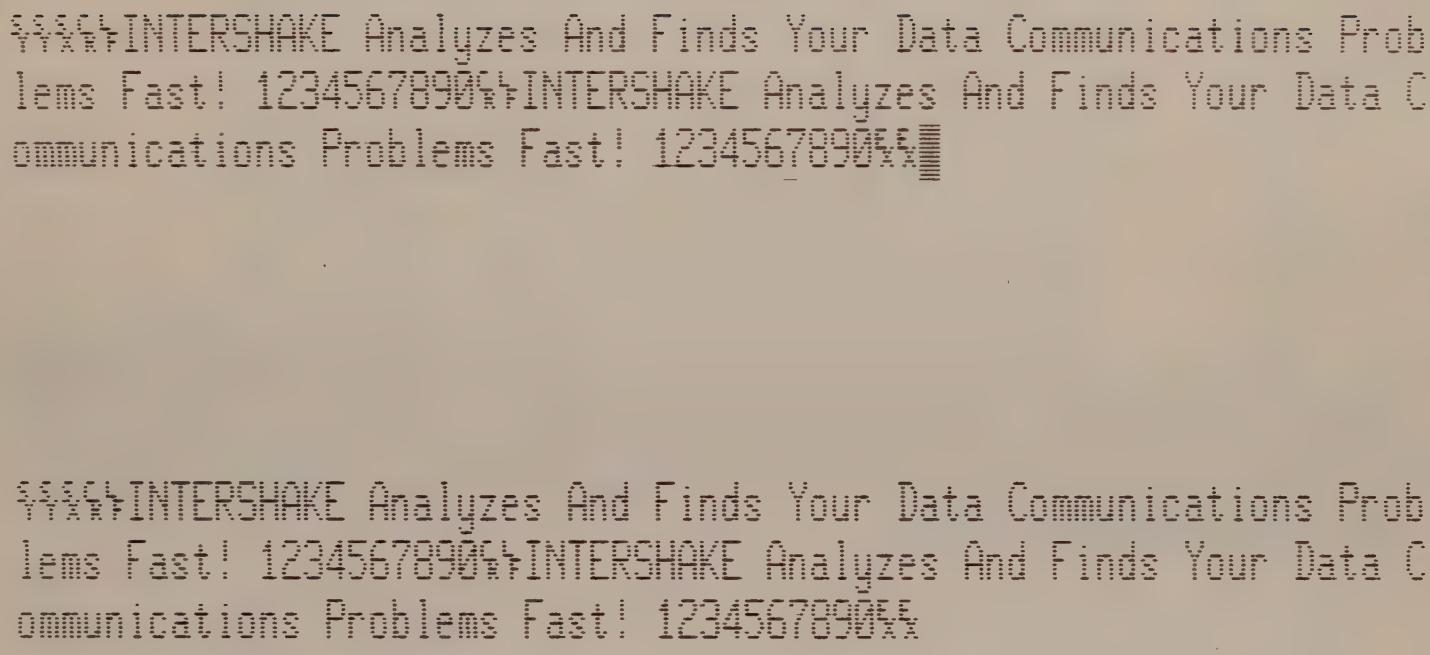

%%%%↓INTERSHAKE Analyzes And Finds Your Data Communications Prob
lems Fast! 1234567890%↓INTERSHAKE Analyzes And Finds Your Data C
ommunications Problems Fast! 1234567890%%
%%%%↓INTERSHAKE Analyzes And Finds Your Data Communications Prob
lems Fast! 1234567890%↓INTERSHAKE Analyzes And Finds Your Data C
ommunications Problems Fast! 1234567890%%

FIGURE 3-7 INTERVIEW display showing two outbound data blocks only — no received data. Possible causes: (1) carrier on but loopback not made; (2) garbled data — synchronization cannot be established.

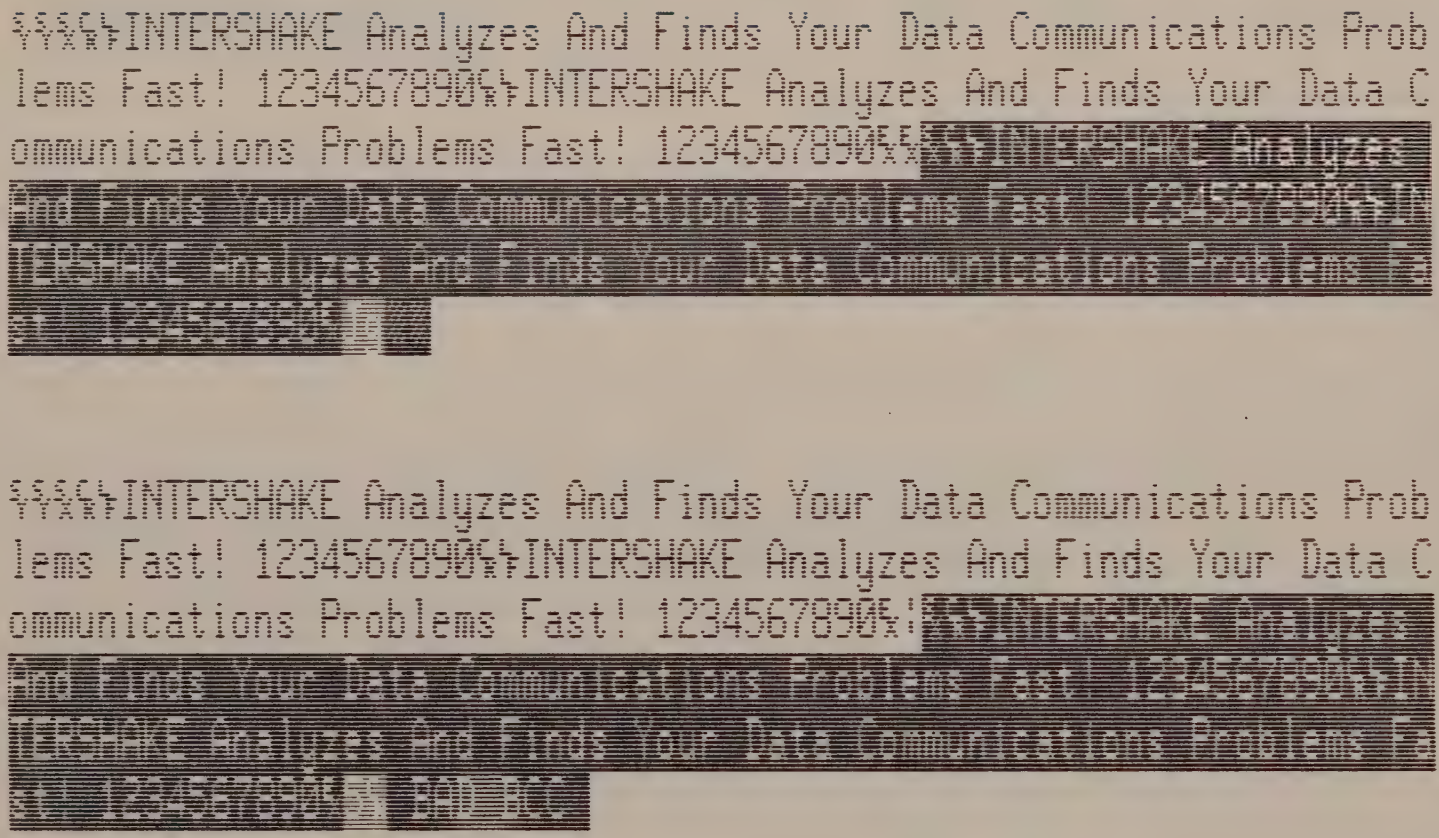


FIGURE 3-8 INTERVIEW display for Self-Test program showing one bad block. Length switch set to 10 blocks.

The program uses the INTERSHAKE timeout interrupt system to indicate lost data, that is, nonreceipt of STX or ETX. Lost data may indicate link problems or that loopback is not established correctly. Received parity error characters will be displayed on the INTERVIEW in reverse half-intensity. Upon receipt of an ETX the program tests CRC. The first CRC error detected will be displayed on Page 2 of the INTERVIEW; the second CRC error, on Page 1.

3.6 Errors and Displays

1. Normally, the display of each transmit block is followed, in reverse full-intensity video, by the same block as it is received through the receive delay line (see Fig. 3-3).
2. If modem conditioning, RLSD, is OFF, "RLSD OFF" appears on the INTERVIEW (see Fig. 3-6).
3. An RLSD hit (carrier dropout) causes the appropriate block to be captured and the alarm to beep 6 times. Should RLSD stay off, the modem is retested. The INTERVIEW displays the message "RLSD OFF" (Fig. 3-6). Each time RLSD goes OFF, an FF_{16} is inserted into results memory.
4. If only one error occurs, that error appears on Page 2 of the INTERVIEW and the last good block is displayed on Page 1 for comparison.
5. If two or more errors occur, the first is displayed on Page 2; the second, on Page 1 (see Fig. 3-4).
6. Only a block errored as a direct result of CRC error is accompanied by a "BAD BCC" message.
7. Display of only transmit data on both Pages 1 and 2 indicates an open loopback or the inability to establish synchronization on the receive block (see Fig. 3-7).
8. The same display can be obtained if RLSD hits occur during transmit time. Under this condition the vectored interrupt takes the program through the error recovery routine and deletes any received data. In testing a communications link, the program gives priority to recording or indicating RLSD dropouts (line problems).
9. BCC characters are indicated in half-intensity.

n interactive test: com-
..... ve disabled to run it.

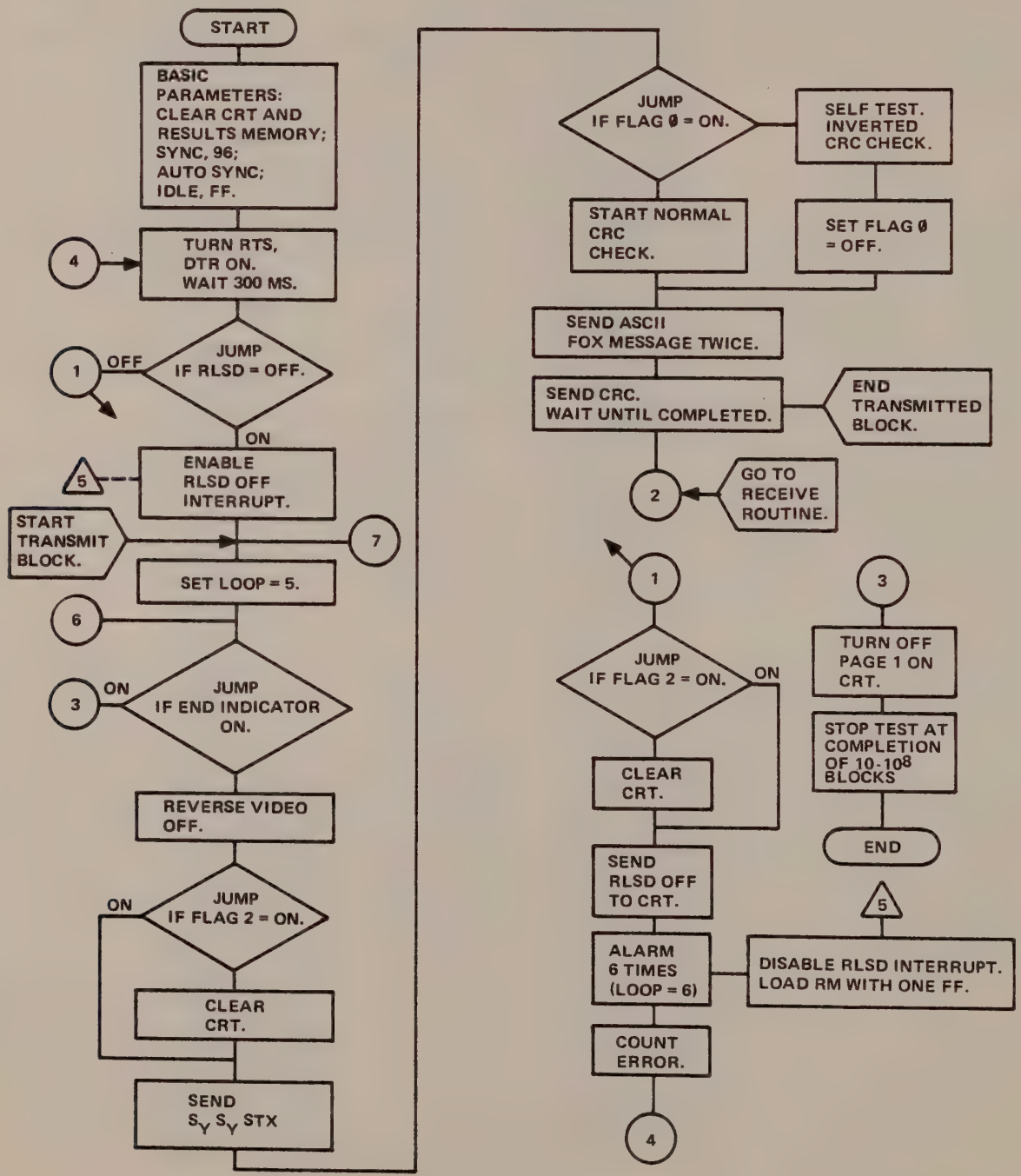
See Appendix B for the INTERSHAKE control panel zones.

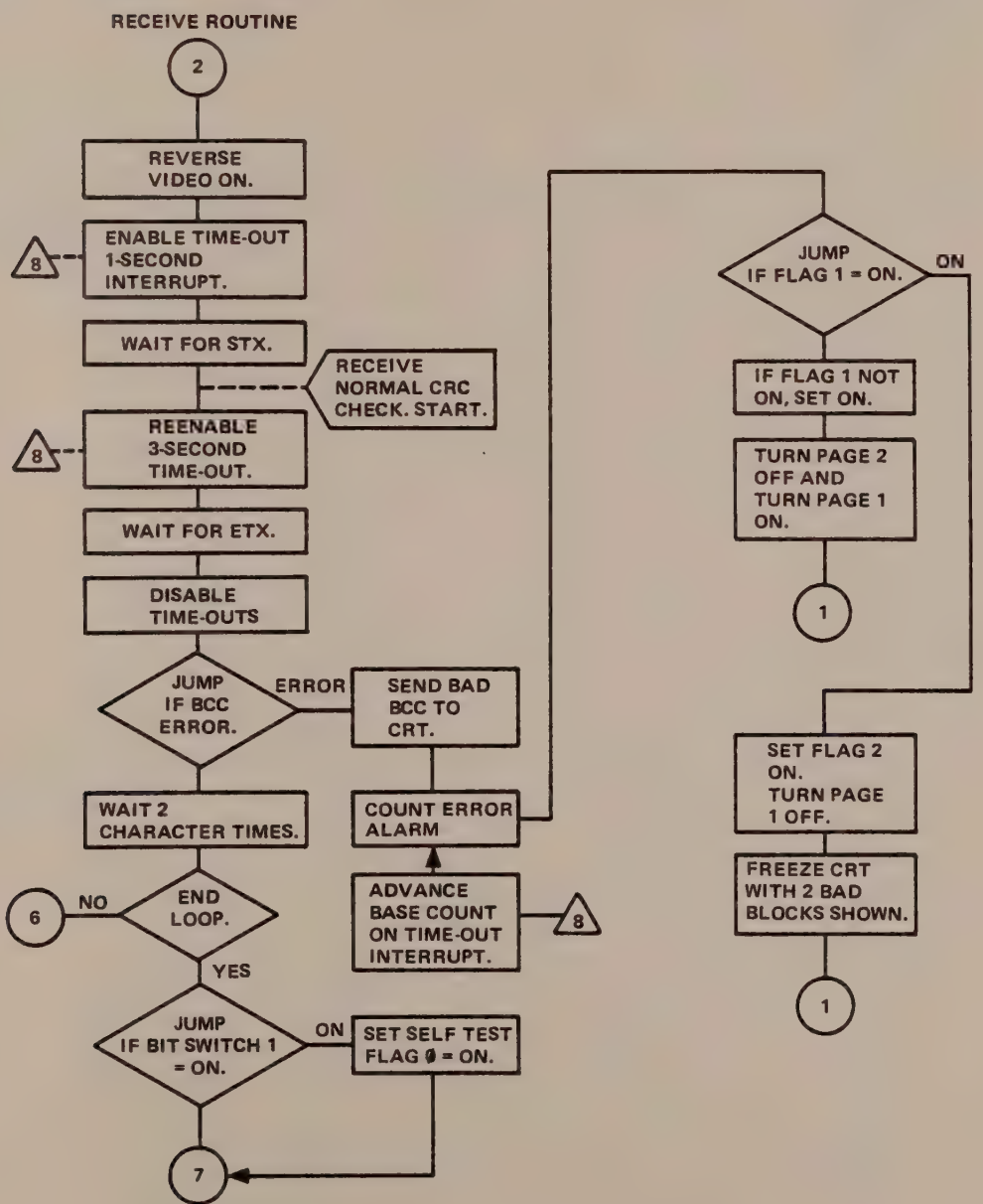
1. Select PROM cell or load program for running (see Section 1).
2. External clock (zone 1) (modem supplies clock when system is on line).
3. Synchronous operation (zone 1).
4. 7 information bits (zone 1).
5. EVEN parity (zone 1).
6. Select TEST MODEM (zone 3).
7. RS-232 toggle switches (zone 5) RTS and DTR to (7X) position (under program control). All others to THRU.
8. Counter input (zone 6) to EVENTS (10X).
9. Counter range switch (zone 6) to 10 - 10^8, depending on number of blocks to be sent.
10. Connect DTM-2 to modem via modem connector.
11. Be sure self test is off:
    For Series A through E units, the instruction at program address BD_{16} (0106) must be edited to an 0298 No-op instruction. (Series A through E units cannot perform Function 06.) In Series F and higher units, Bit switch 1 must be off.
12. Depress STEP (zone 3).

3.8 Off-Line Self Test or System Demonstration

1. Do steps 1 and 3 through 9 of the on-line setup. Select operating speed 1200 bps or higher.
2. For Series A through E units, edit step BD_{16} (0106) to 0147 to enable the self test. (Series A through E units cannot perform Function 06.)
3. Run a patch cord from the + 12V test point (zone 2) to pin 8, RLSD RS-232 test point (zone 5). RTS coming on will enable RLSD.
4. Place MON SIGS OUT toggle switch (zone 3) in MON SIGS OUT position (DTM-2 loopback).
5. Depress STEP (zone 3).

3.9 Program Flow Diagram




RECEIVE ROUTINE
2
REVERSE VIDEO ON.
8
ENABLE TIME-OUT 1-SECOND INTERRUPT.
WAIT FOR STX.
RECEIVE NORMAL CRC CHECK. START.
8
REENABLE 3-SECOND TIME-OUT.
WAIT FOR ETX.
DISABLE TIME-OUTS
JUMP IF BCC ERROR.
ERROR
SEND BAD BCC TO CRT.
WAIT 2 CHARACTER TIMES.
COUNT ERROR ALARM
6
NO
END LOOP.
ADVANCE BASE COUNT ON TIME-OUT INTERRUPT.
8
YES
JUMP IF BIT SWITCH 1 = ON.
ON
SET SELF TEST FLAG 0 = ON.
7
JUMP IF FLAG 1 = ON.
ON
IF FLAG 1 NOT ON, SET ON.
TURN PAGE 2 OFF AND TURN PAGE 1 ON.
1
SET FLAG 2 ON. TURN PAGE 1 OFF.
FREEZE CRT WITH 2 BAD BLOCKS SHOWN.
1

3.10 Program

INTERSHAKE II PROGRAM

TITLE: CRC LOOPBACK

FILE NO. D04A
SHEET 1 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 4 (0)	0	0	01	94		
	1	1	00	94	Clear CRT.	
	2	2	02	80		
	3	3	21	94	Select Page 2.	
	4	4	75	42	Loop 75 times.	
	5	5	A0	50	Send space. (Send 75 spaces.)	
	6	6	05	41	Load address register.	
	7	7	00	43	End loop.	
	8	8	C3	50	Send C.	
	9	9	D2	50	Send R.	
	A	10	C3	50	Send C.	
	B	11	A0	50	Send space.	
	C	12	D4	50	Send T.	
	D	13	C5	50	Send E.	
	E	14	53	50	Send S.	
	F	15	D4	50	Send T.	
D 9 5 (1)	0	16	2E	50	Send period.	
	1	17	A0	50	Send space.	
	2	18	72	42		
	3	19	A0	50		
	4	20	13	41	Send 72 spaces.	
	5	21	00	43		
	6	22	A0	50	Send space.	
	7	23	A0	50	Send space.	
	8	24	A0	50	Send space.	
	9	25	50	50	Send P.	
	A	26	41	50	Send A.	
	B	27	D4	50	Send T.	
	C	28	C3	50	Send C.	
	D	29	48	50	Send H.	
	E	30	A0	50	Send space.	
	F	31	2B	50	Send +.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE: ASCII
SPEED: —
ASYNC / (SYNC)
SYN CHARACTER: 96
STOP BIT: 1.0 , 1.5 , 2.0
INFO BITS: 5 , 6 , (7) , 8
PARITY: NONE , ODD , (EVEN)
CONTROL EIA / (OFF)
ON-LINE: TD/RD , TD , RD
OFF-LINE: TERM / (MODEM)
(MON SIGS / NORMAL)
PATCH CORDS: Self test Loop Back +12 to RLSD
CONTROL EIA (V.24): RTS 7X DTR 7X
COUNTER ZONE: Base Count 10X 10^0 - 10^8 Length
INTERRUPTS: RLSD
FLAGS:
LATCH:

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A 6 2	0	32	B1	50	Send 1.	
	1	33	B2	50	Send 2.	
	2	34	A0	50	Send space.	
	3	35	74	50	Send t.	
	4	36	6F	50	Send o.	
	5	37	A0	50	Send space.	
	6	38	D2	50	Send R.	
	7	39	CC	50	Send L.	
	8	40	53	50	Send S.	
	9	41	44	50	Send D.	
	A	42	AC	50	Send ,.	
	B	43	A0	50	Send space.	
	C	44	C3	50	Send C.	
	D	45	6F	50	Send o.	
	E	46	F5	50	Send u.	
	F	47	EE	50	Send n.	
F B 7 3	0	48	74	50	Send t.	
	1	49	65	50	Send e.	
	2	50	72	50	Send r.	
	3	51	A0	50	Send space.	
	4	52	69	50	Send i.	
	5	53	EE	50	Send n.	
	6	54	F0	50	Send p.	
	7	55	5F	50	Send u.	
	8	56	74	50	Send t.	
	9	57	74	50	Send t.	
	A	58	6F	50	Send o.	
	B	59	A0	50	Send space.	
	C	60	B1	50	Send 1.	
	D	61	30	50	Send 0.	
	E	62	D8	50	Send X.	
	F	63	2E	50	Send period.	

FILE NO. D04A
SHEET 18 OF 4
PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 2 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 (4) 0	0	0	A0	50	Send space.	
	1	1	A0	50	Send space.	
	2	2	A0	50	Send space.	
	3	3	A0	50	Send space.	
	4	4	A0	50	Send space.	
	5	5	A0	50	Send space.	
	6	6	51	42	} Send 51 spaces.	
	7	7	A0	50		
	8	8	47	41		
	9	9	00	43		
	A	10	53	50	Send S.	
	B	11	59	50	Send Y.	
	C	12	4E	50	Send N.	
	D	13	C3	50	Send C.	
	E	14	A0	50	Send space.	
	F	15	B7	50	Send 7.	
D 9 (5) 1	0	16	A0	50	Send space.	
	1	17	E2	50	Send b.	
	2	18	69	50	Send i.	
	3	19	74	50	Send t.	
	4	20	A0	50	Send space.	
	5	21	65	50	Send e.	
	6	22	F6	50	Send v.	
	7	23	65	50	Send e.	
	8	24	EE	50	Send n.	
	9	25	A0	50	Send space.	
	A	26	F0	50	Send p.	
	B	27	E1	50	Send a.	
	C	28	72	50	Send r.	
	D	29	69	50	Send i.	
	E	30	74	50	Send t.	
	F	31	F9	50	Send y.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

- CODE
- SPEED
- ASYNC / SYNC
- SYN CHARACTER
- STOP BIT 1.0 , 1.5 , 2.0
- INFO BITS 5 , 6 , 7 , 8
- PARITY NONE , ODD , EVEN
- CONTROL EIA / OFF
- ON-LINE TD/RD , TD , RD
- OFF-LINE TERM / MODEM
- MON SIGS / NORMAL
- PATCH CORDS
- CONTROL EIA (V.24)
- COUNTER ZONE
- INTERRUPTS
- FLAGS
- LATCH

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP
E A (6) 2	0	32	AC	50	Send ,.	
	1	33	A0	50	Send space.	
	2	34	4D	50	Send M.	
	3	35	6F	50	Send o.	
	4	36	EE	50	Send n.	
	5	37	A0	50	Send space.	
	6	38	F3	50	Send s.	
	7	39	69	50	Send i.	
	8	40	E7	50	Send g.	
	9	41	F3	50	Send s.	
	A	42	6F	50	Send o.	
	B	43	F5	50	Send u.	
	C	44	74	50	Send t.	
	D	45	A0	50	Send space.	
	E	46	6F	50	Send o.	
	F	47	EE	50	Send n.	
F B (7) 3	0	48	2E	50	Send period.	
	1	49	57	42	Send 57 spaces.	
	2	50	A0	50		
	3	51	72	41		
	4	52	00	43		
	5	53	50	50	Send P.	
	6	54	41	50	Send A.	
	7	55	47	50	Send G.	
	8	56	C5	50	Send E.	
	9	57	A0	50	Send space.	
	A	58	B1	50	Send 1.	
	B	59	2B	50	Send +.	
	C	60	B2	50	Send 2.	
	D	61	A0	50	Send space.	
	E	62	A6	50	Send &.	
	F	63	A0	50	Send space.	

FILE NO. D04A
SHEET 2B OF 4
PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME:

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 3 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 (2) 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C (8) 4 0	0	0	50	50	Send P.	
	1	1	D2	50	Send R.	
	2	2	C5	50	Send E.	
	3	3	53	50	Send S.	
	4	4	53	50	Send S.	
	5	5	A0	50	Send space.	
	6	6	53	50	Send S.	
	7	7	D4	50	Send T.	
	8	8	C5	50	Send E.	
	9	9	50	50	Send P.	
	A	10	31	94	Freeze CRT.	
	B	11	00	00	Halt. Wait for step button.	
	C	12	30	94	Unfreeze CRT.	
	D	13	6C	94	Half-intensity on parity error.	
	E	14	96	90	Sync character = 96_{16}.	
	F	15	12	95	Auto sync on.	
D (9) 5 1	0	16	04	96	2K Delay line on.	
	1	17	FF	57	Send fill character.	
	2	18	88	70	Turn RTS and DTR on.	
	3	19	03	82	Wait 300 ms.	
	4	20	E7	41	Load address register.	
	5	21	10	78	Jump if RLSD off.	
	6	22	10	75	Enable interrupt on; RLSD off.	
	7	23	05	42	Set test loop = 5.	
	8	24	F9	41	Load address register.	
	9	25	B3	47	Jump if end count on.	
	A	26	50	94	Reverse video off.	
	B	27	A0	41	Load address register.	
	C	28	23	47	Jump if Flag 2 = 1 or on.	
	D	29	01	94	} Clear CRT.	
	E	30	20	80		
	F	31	00	94		

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

- CODE
- SPEED
- ASYNC / SYNC
- SYN CHARACTER
- STOP BIT 1.0 , 1.5 , 2.0
- INFO BITS 5 , 6 , 7 , 8
- PARITY NONE , ODD , EVEN
- CONTROL EIA / OFF
- ON-LINE TD/RD , TD , RD
- OFF-LINE TERM / MODEM
- MON SIGS / NORMAL
- PATCH CORDS
- CONTROL EIA (V.24)
- COUNTER ZONE
- INTERRUPTS
- FLAGS
- LATCH

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 (2) 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E (A) 6 2	0	32	96	50	Send sync 96_{16}.	
	1	33	96	50	Send sync 96_{16}.	
	2	34	82	50	Send STX.	
	3	35	A7	41	Load address register.	
	4	36	03	47	Jump if Flag 0 = 1.	
	5	37	00	58	Start CRC-16 Calculation.	
	6	38	A9	40	Go-to.	
	7	39	10	58	Start inverted CRC-16 calculation.	
	8	40	00	47	Set Flag 0 = 0.	
	9	41	02	61	Send ASCII message 2 times.	
	A	42	03	50	Sent ETX.	
	B	43	00	59	Send CRC.	
	C	44	00	15	Wait until TX is complete.	
	D	45	51	94	Reverse video on.	
	E	46	10	84	Set time-out interrupt to 1 sec.	
	F	47	0C	97	Enable time-out interrupt.	
F (B) 7 3	0	48	82	16	Wait for STX.	
	1	49	08	97	Disable time-out.	
	2	50	00	38	Start receive CRC-16 normal calculation.	
	3	51	30	84	Set time-out interrupt to 3 sec.	
	4	52	0C	97	Enable time-out interrupt.	
	5	53	03	16	Wait for ETX.	
	6	54	08	97	Disable interrupt.	
	7	55	C1	41	Load address register.	
	8	56	00	39	Test for CRC error.	
	9	57	24	83	Wait 24 bit times.	
	A	58	98	41	Load address register.	
	B	59	00	43	End test loop (5 times).	
	C	60	BF	41	Load address register.	
	D	61	01	06	Jump if bit switches = 01_{16}.	
	E	62	97	40	Go-to.	
	F	63	01	47	Set Flag 0 = 1.	

FILE NO. D04A
SHEET 3B OF 4
PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 4 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) ③ 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
Ⓒ 8 4 0	0	0	97	40	Go-to.	
	1	1	71	94	Blink CRT on.	
	2	2	A0	50	Send space.	
	3	3	42	50	Send B.	
	4	4	41	50	Send A.	
	5	5	44	50	Send D.	
	6	6	A0	50	Send space.	
	7	7	42	50	Send B.	
	8	8	C3	50	Send C.	
	9	9	C3	50	Send C.	
	A	10	A0	50	Send space.	
	B	11	70	94	Blink CRT off.	
	C	12	08	97	Disable interrupt time-out.	
	D	13	03	87	Add 1 to counter.	
	E	14	01	70	Alarm on.	
	F	15	03	81	Delay 30 ms.	
Ⓓ 9 5 1	0	16	01	71	Alarm off.	
	1	17	D8	41	Load address register.	
	2	18	13	47	Jump if Flag 1 = 1.	
	3	19	11	47	Set Flag 1 = 1.	
	4	20	20	82	Wait 2 seconds.	
	5	21	20	94	Select Page 2 off.	
	6	22	11	94	Select Page 1 on.	
	7	23	92	40	Go-to.	
	8	24	21	47	Jump if Flag 2 = 1.	
	9	25	10	94	Select Page 1 off.	
	A	26	31	94	Freeze CRT.	
	B	27	92	40	Go-to.	
	C	28	00	76	Disable RLSD interrupt.	
	D	29	FF	07	Load fill character.	
	E	30	06	42	Loop 6 times.	
	F	31	01	70	Beep 6 times.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE

SPEED

ASYNC / SYNC

SYN CHARACTER

STOP BIT
1.0 , 1.5 , 2.0

INFO BITS
5 , 6 , 7 , 8

PARITY
NONE , ODD , EVEN

CONTROL EIA / OFF

ON-LINE
TD/RD , TD , RD

OFF-LINE
TERM / MODEM

MON SIGS / NORMAL

PATCH CORDS

CONTROL EIA (V.24)

COUNTER ZONE

INTERRUPTS

FLAGS

LATCH

CONTINUE ON OTHER SIDE

CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A 6 2	0	32	03	81	Wait 30 ms.	
	1	33	01	71	Turn alarm off.	
	2	34	03	81	Wait 30 ms.	
	3	35	DF	41	Load address register.	
	4	36	00	43	End loop.	
	5	37	03	87	Add 1 to event count.	
	6	38	92	40	Go-to.	
	7	39	EC	41	Load address register.	
	8	40	23	47	Jump if Flag 2 = 1.	
	9	41	01	94	} Clear CRT.	
	A	42	20	80		
	B	43	00	94		
	C	44	51	94	Reverse video on.	
	D	45	A0	50	Send space.	
	E	46	D2	50	Send R.	
	F	47	CC	50	Send L.	
F B 7 3	0	48	53	50	Send S.	
	1	49	44	50	Send D.	
	2	50	A0	50	Send space.	
	3	51	CF	50	Send O.	
	4	52	C6	50	Send F.	
	5	53	C6	50	Send F.	
	6	54	A0	50	Send space.	
	7	55	50	94	Reverse video off.	
	8	56	DE	40	Go-to.	
	9	57	10	94	Page 1 select off.	
	A	58	00	99	End.	
	B	59	00	00	Halt.	
	C	60	DC	40	Go-to.	
	D	61	00	85	Add 1 to base count.	
	E	62	CC	40	Go-to.	
	F	63	00	00	Halt.	

FILE NO. D04A
SHEET 4B OF 4
PROGRAM LOCATION
DTM S/N
CELL C-D
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: John A. Mansker DATE
COMPANY NAME: Atlantic Research Corporation. TEL. NO.
ADDRESS:

FORM NO. TP-139-6-77

3.11 Inter-KEY Program Listing

```
Cg
0194 AUX  A050 XMT  5050 XMT  9740 JMP
0094 AUX  A050 XMT  D250 XMT  7194 AUX
0280 DLY  A050 XMT  C550 XMT  A050 XMT
2194 AUX  A050 XMT  5350 XMT  4250 XMT
7542 PRE  A050 XMT  5350 XMT  4150 XMT
A050 XMT  A050 XMT  A050 XMT  4450 XMT
0541 PRE  5142 PRE  5350 XMT  A050 XMT
0043 JEL  A050 XMT  D450 XMT  4250 XMT

C350 XMT  4741 PRE  C550 XMT  C350 XMT
D250 XMT  0043 JEL  5050 XMT  C350 XMT
C350 XMT  5350 XMT  3194 AUX  A050 XMT
A050 XMT  5950 XMT  0000 HLT  7094 AUX
D450 XMT  4E50 XMT  3094 AUX  0897 INT
C550 XMT  C350 XMT  6C94 AUX  0387 CTR
5350 XMT  A050 XMT  9690 SYN  0170 232
D450 XMT  B750 XMT  1295 SYN  0381 DLY

2E50 XMT  A050 XMT  0496 AUT  0171 232
A050 XMT  E250 XMT  FF57 xmt  D841 PRE
7242 PRE  6950 XMT  8870 232  1347 JFG
A050 XMT  7450 XMT  0382 DLY  1147 FLG
1341 PRE  A050 XMT  E741 PRE  2082 DLY
0043 JEL  6550 XMT  1078 JID  2094 AUX
A050 XMT  F650 XMT  1075 INT  1194 AUX
A050 XMT  6550 XMT  0542 PRE  9240 JMP

A050 XMT  EE50 XMT  F941 PRE  2147 FLG
5050 XMT  A050 XMT  B347 JFG  1094 AUX
4150 XMT  F050 XMT  5094 AUX  3194 AUX
D450 XMT  E150 XMT  A041 PRE  9240 JMP
C350 XMT  7250 XMT  2347 JFG  0076 INT
4850 XMT  6950 XMT  0194 AUX  FF07 BSW
A050 XMT  7450 XMT  2080 DLY  0642 PRE
2B50 XMT  F950 XMT  0094 AUX  0170 232

B150 XMT  AC50 XMT  9650 XMT  0381 DLY
B250 XMT  A050 XMT  9650 XMT  0171 232
A050 XMT  4D50 XMT  8250 XMT  0381 DLY
7450 XMT  6F50 XMT  A741 PRE  DF41 PRE
6F50 XMT  EE50 XMT  0347 JFG  0043 JEL
A050 XMT  A050 XMT  0058 BCC  0387 CTR
D250 XMT  F350 XMT  A940 JMP  9240 JMP
CC50 XMT  6950 XMT  1058 BCC  EC41 PRE

5350 XMT  E750 XMT  0047 FLG  2347 JFG
4450 XMT  F350 XMT  0261 MSG  0194 AUX
AC50 XMT  6F50 XMT  0350 XMT  2080 DLY
A050 XMT  F550 XMT  0059 BCC  0094 AUX
C350 XMT  7450 XMT  0015 DLY  5194 AUX
6F50 XMT  A050 XMT  5194 AUX  A050 XMT
F550 XMT  6F50 XMT  1084 INT  D250 XMT
EE50 XMT  EE50 XMT  0C97 INT  CC50 XMT

7450 XMT  2E50 XMT  8216 TRP  5350 XMT
6550 XMT  5742 PRE  0897 INT  4450 XMT
7250 XMT  A050 XMT  0038 BCC  A050 XMT
A050 XMT  7241 PRE  3084 INT  CF50 XMT
6950 XMT  0043 JEL  0C97 INT  C650 XMT
EE50 XMT  5050 XMT  0316 TRP  C650 XMT
F050 XMT  4150 XMT  0897 INT  A050 XMT
F550 XMT  4750 XMT  C141 PRE  5094 AUX

7450 XMT  C550 XMT  0039 JBE  DE40 JMP
7450 XMT  A050 XMT  2483 DLY  1094 AUX
6F50 XMT  B150 XMT  9841 PRE  0099 END
A050 XMT  2B50 XMT  0043 JEL  0000 HLT
B150 XMT  B250 XMT  BF41 PRE  DC40 JMP
3050 XMT  A050 XMT  0106 JSW  0085 CTR
D850 XMT  A650 XMT  9740 JMP  CC40 JMP
2E50 XMT  A050 XMT  0147 FLG  0000 HLT
s$
```

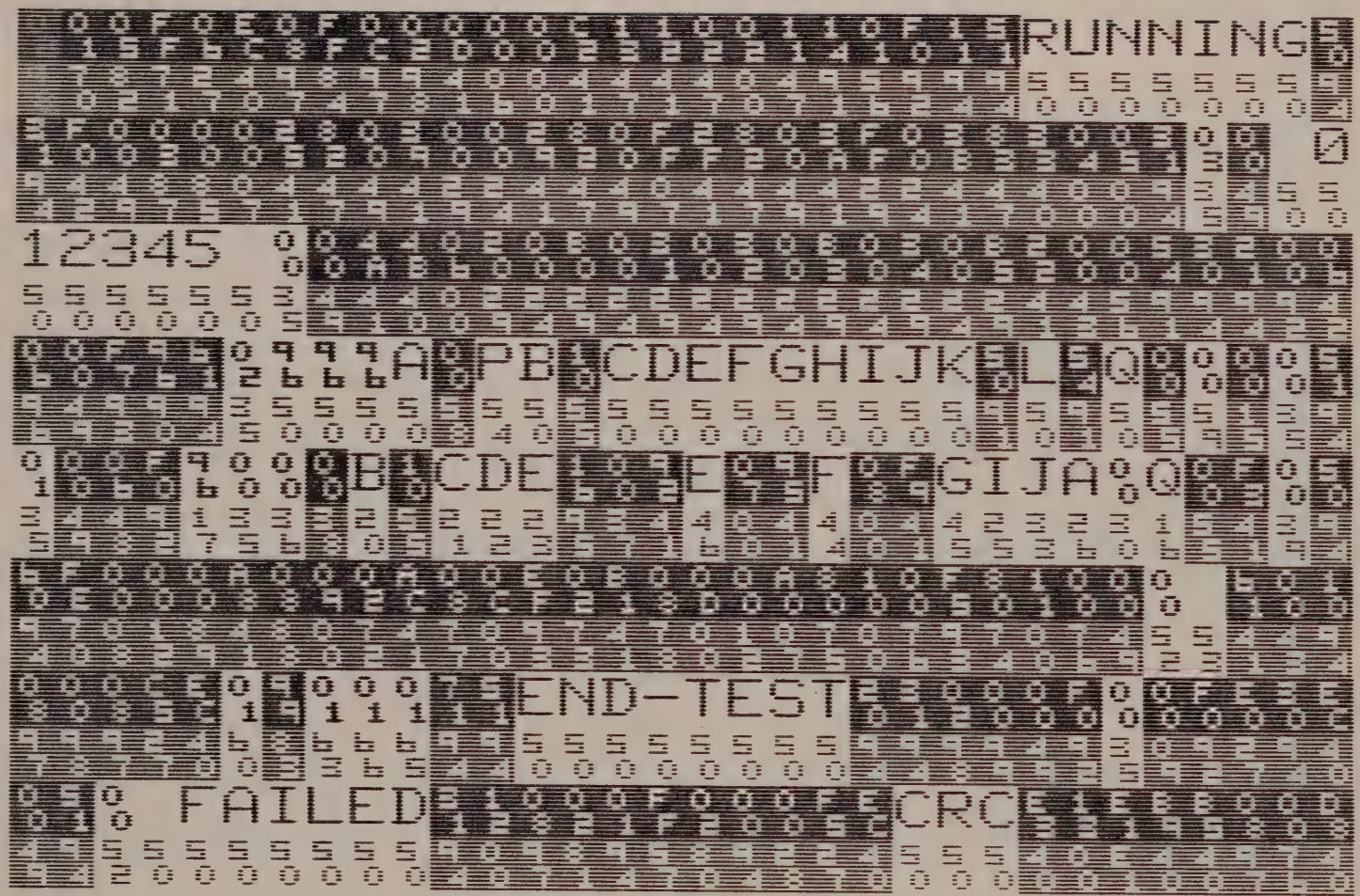


FIGURE 4-1 LOAD mode display of Self-Test program. (Note: This display will not be seen unless the operator calls it.)

4 INTERSHAKE Self Test (Cell E-F)

4.1 Panel Setup

Set up the INTERSHAKE and INTERVIEW panels as follows (see Appendix B):

Panel Zone	*Setting or Patch*
5	All RS-232 switches OFF (7X)
3	CONTROL EIA switch OFF
8	Bit switches to SPACE (off)
2	Patch CONTROL OUT to MONITOR IN
2,5	Patch DETECT IN to RTS input
5	Patch Pin 24 to Pin 17
—	Loop modem connector to terminal connector with 25-pin cable.
6	Set COUNTER input switch to EVENTS (8X)
—	All other DTM-2 panel switches: Don't care
INTERVIEW	Set PAGE to 1 and 2
INTERVIEW	Set CODE to ASCII
4	Depress RUN button
3	Press MARK and SPACE buttons; and then START

4.2 Modification M550/555

All Function 92 instructions must be replaced with No-op instructions, 0298. Speed must be set manually to 9600 bps.

4.3 Test Operation

The Self-Test program listing as displayed on the INTERVIEW in LOAD mode is shown in Figure 4-1.

Proper operation of the self test starts with a 0.5-second audible alarm test and display of the message RUNNING (Figure 4-2) on the CRT after the screen is cleared. The cursor is located at the end of the message.

While the results memory is being tested, the CRT is frozen. The freeze is removed when the loopback synchronization test starts. A specific sequence of characters is transmitted (and displayed in normal half-intensity video). The same block is checked for both sequence order and CRC. Specific characters of the block are simultaneously recorded into results memory along with loop count, RS-232 lead status, and counter reading (15). After a successful sequence and CRC test, the recorded data is read from results memory to the CRT for visual observation. (See Figure 4-3.)

After proper completion of both the results memory test and the loopback-sequence-CRC test, a Function 0098 recycle test is executed. This restarts the test, which is marked by a second 0.5-second Beep from the audible alarm. However, Flag 1 should now be set, causing the program to turn Page 1 off, Page 2 on, and send four stored messages in ASCII, EBCDIC, Selectric, and EBCD, respectively. Figures 4-4 through 4-7 show the successive message displays that appear on the INTERVIEW screen for the four codes. Upon completion of the stored messages, an END-TEST message in blinking reverse video appears on the CRT and the program ends in a Function 99. (See Figure 4-3.)

At the end of the loopback test the RS-232 leads are tested for the conditions ON, OFF, Jump if ON, Jump if OFF, Wait until ON, Wait until OFF, Interrupt if ON and Interrupt if OFF. The leads are switched from modem to terminal mode via auto paneling. This takes advantage of the proper housekeeping done on the INTERSHAKE EIA connectors. The patch from CONTROL OUT to MONITOR IN will test the status of the CONTROL OUT test point as well as operation of the hit indicator, if it is reset before the test is started.

4.4 Identification of Errors

The Self-Test has been developed to help the user determine where a failure has occurred. It also indicates when the test is running and has completed.

If the test fails to complete properly, the point at which failure has occurred may be indicated by a message "(char) FAILED" on the CRT. The ASCII hexadecimal equivalent of the character in the FAILED message is the program step that failed.

The test should complete in no more than 20 seconds, but a failure may cause it to halt and hang in error condition indefinitely.

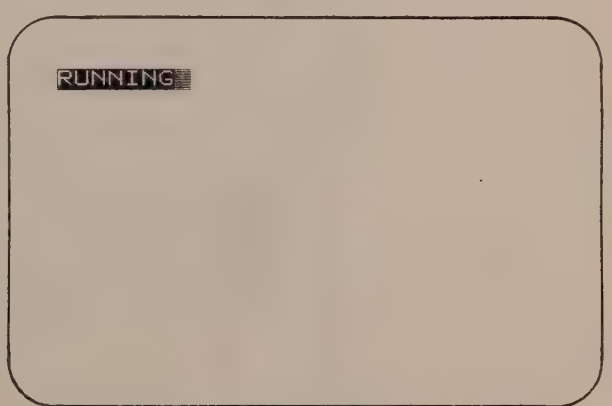


FIGURE 4-2 Upon proper start of the Self Test, this display appears for approximately 10 seconds.

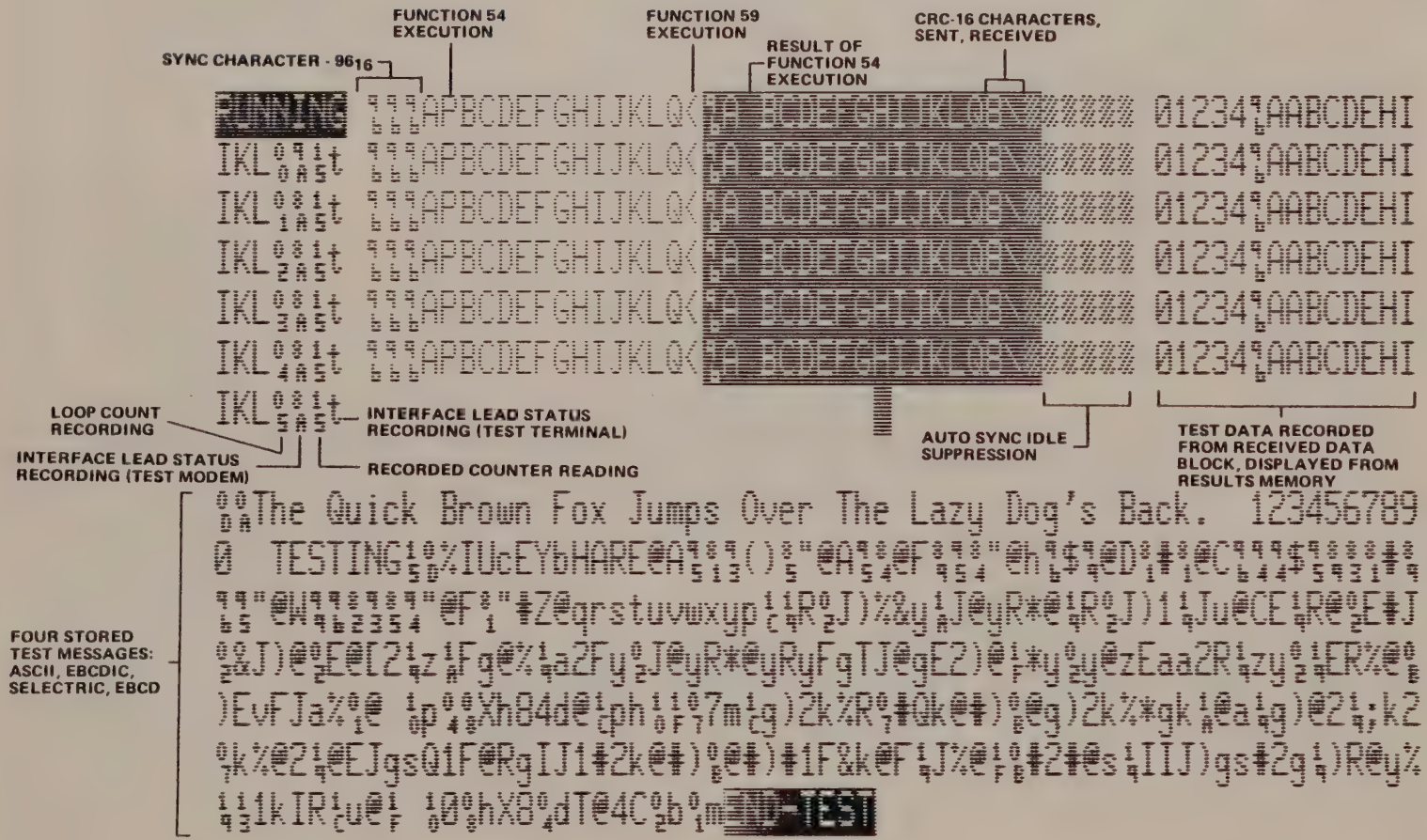

FUNCTION 54 EXECUTION
FUNCTION 59 EXECUTION
CRC-16 CHARACTERS, SENT, RECEIVED
SYNC CHARACTER - 96₁₆
RESULT OF FUNCTION 54 EXECUTION
RUNNING
01234 AABCDEHI
LOOP COUNT RECORDING
INTERFACE LEAD STATUS RECORDING (TEST MODEM)
INTERFACE LEAD STATUS RECORDING (TEST TERMINAL)
RECORDED COUNTER READING
AUTO SYNC IDLE SUPPRESSION
TEST DATA RECORDED FROM RECEIVED DATA BLOCK, DISPLAYED FROM RESULTS MEMORY
FOUR STORED TEST MESSAGES: ASCII, EBCDIC, SELECTRIC, EBCD
The Quick Brown Fox Jumps Over The Lazy Dog's Back. 123456789
TESTING
TEST

FIGURE 4-3 Self-Test data as displayed on INTERVIEW. CRT control character switch in hex position.

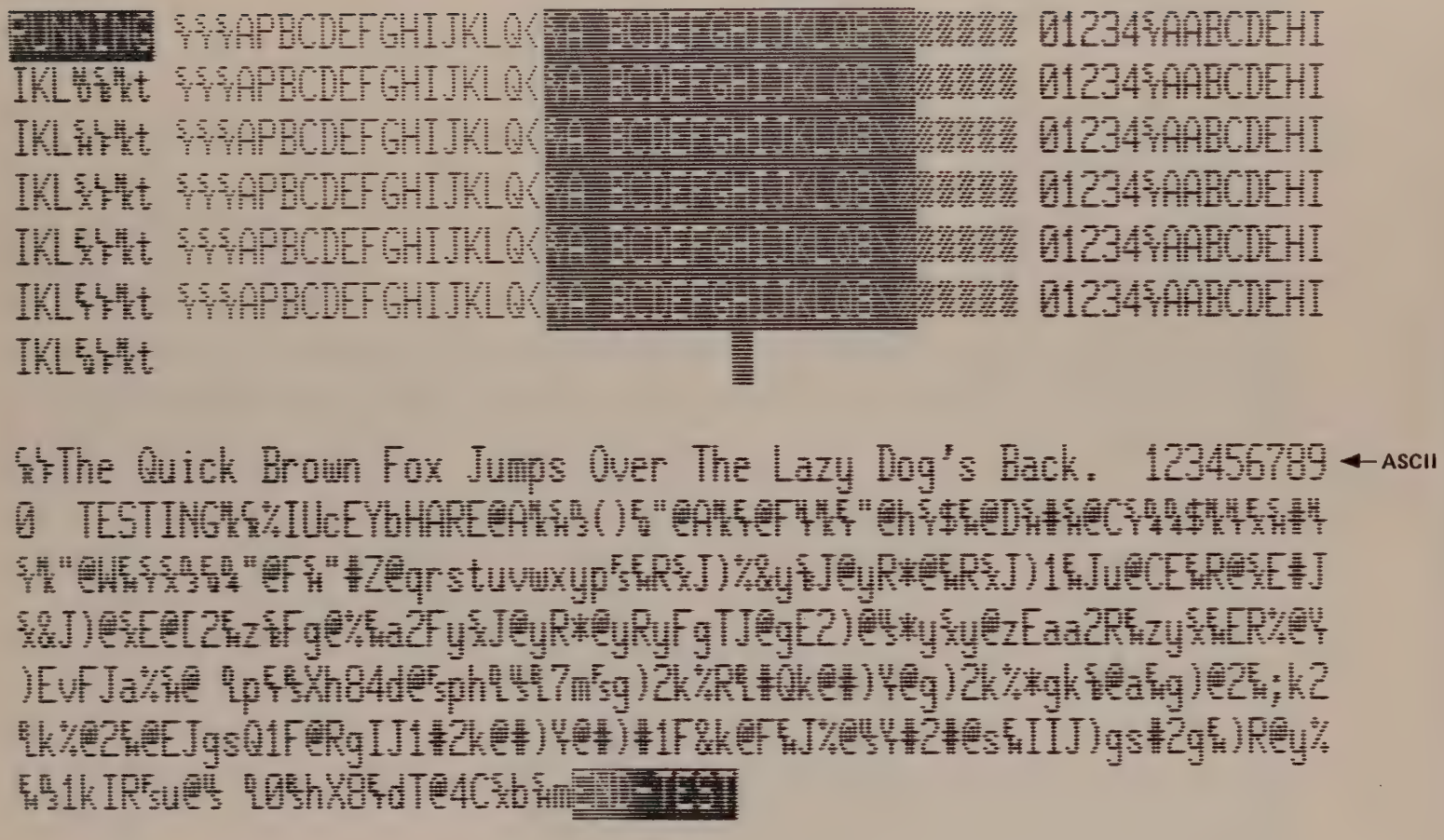


FIGURE 4-4 ASCII message display. The INTERVIEW CONTROL CHAR switch is in the center (mnemonic) position.

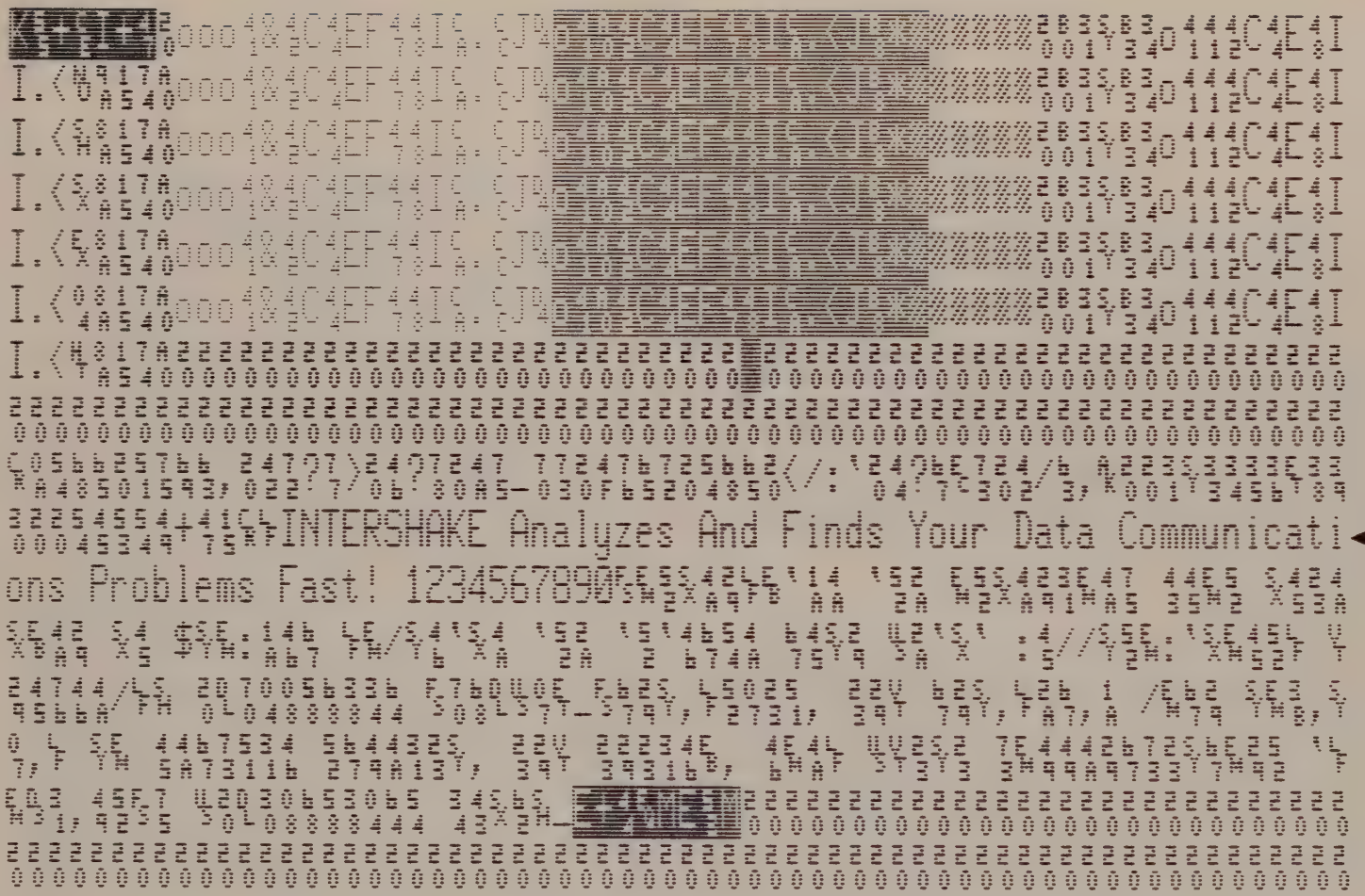


FIGURE 4-5 EBCDIC message display.

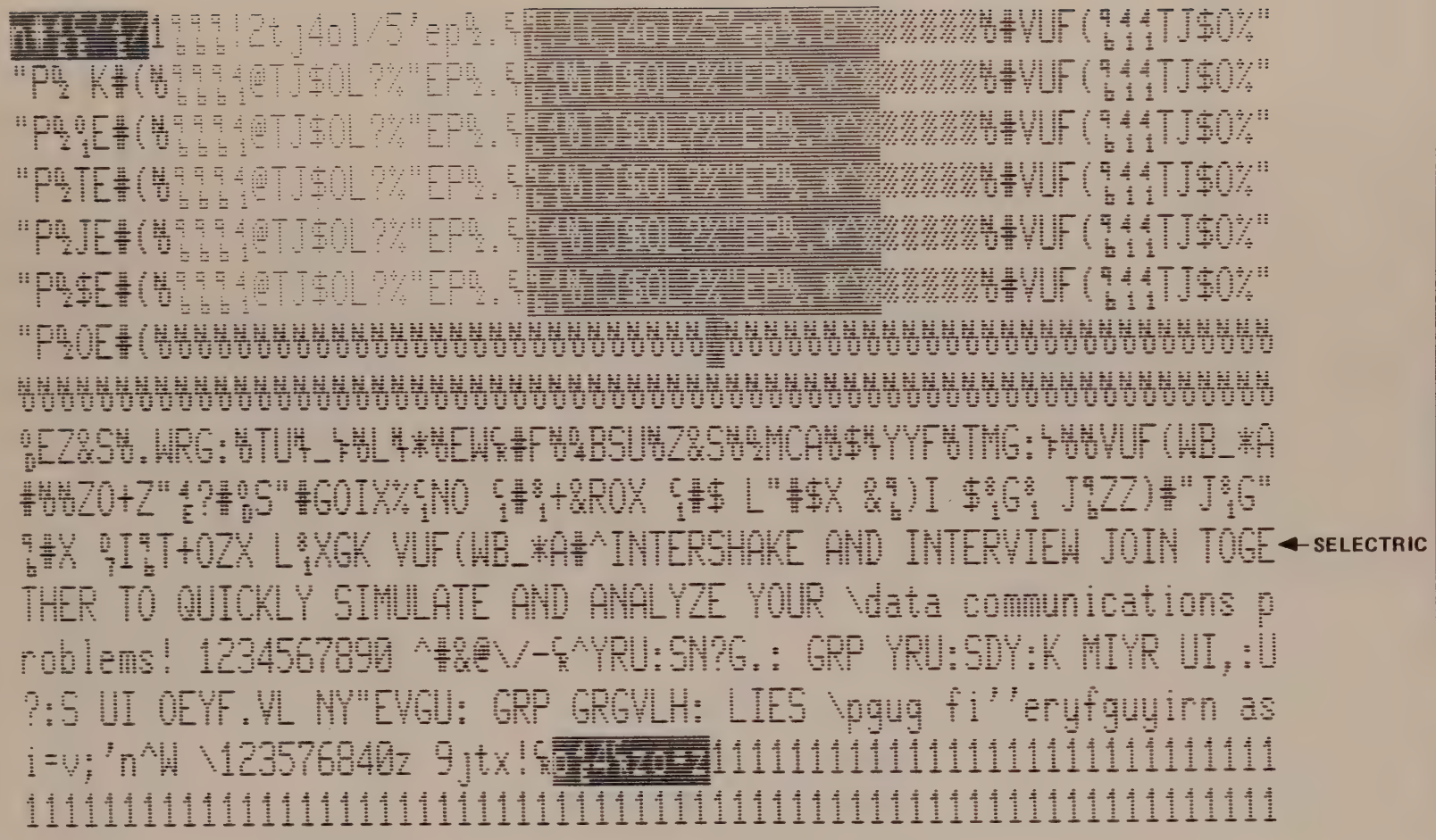

SELECTRIC
INTERSHAKE AND INTERVIEW JOIN TOGE
THER TO QUICKLY SIMULATE AND ANALYZE YOUR \data communications p
roblems! 1234567890 ^#&@\/-¢^YRU:SN?G.: GRP YRU:SDY:K MIYR UI,:U
?:S UI OEYF.VL NY"EVGU: GRP GRGVLH: LIES \pgug fi''eryfguyirn as
i=v;'n^W \123576840z 9jtx!%

FIGURE 4-6 Selectric message display.

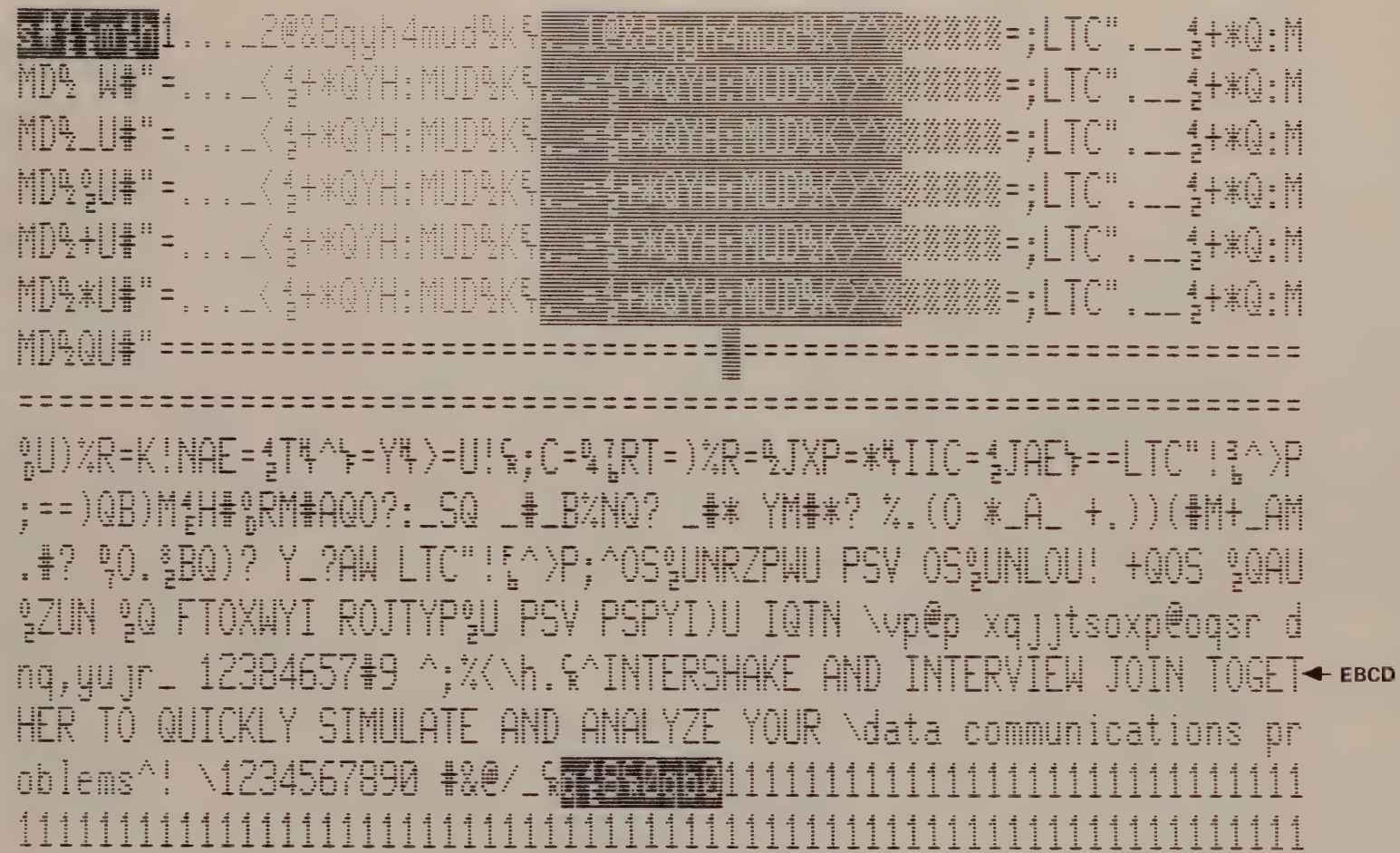


FIGURE 4-7 EBCD message display.

Table 4.1 lists some error indications and their possible causes.

4.5 INTERSHAKE Self-Test Function List

Seventy-four out of the 127 INTERSHAKE II functions appear in the program. They are listed here with comments on their use in this test.

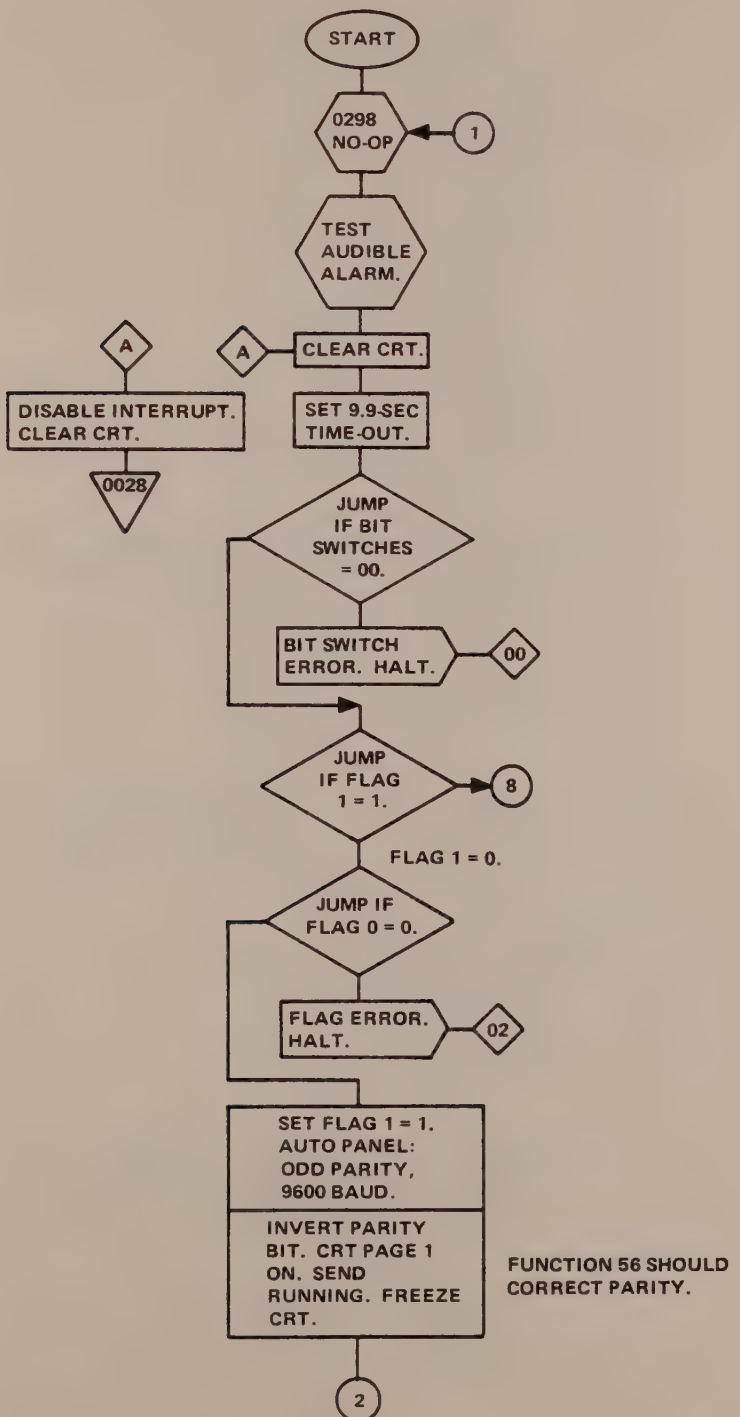
No.	*Description*	*Self-Test Use*
00	Halt	Error halts. Identified by number in the data.
06	Test bit switch and jump	Test bit switches for the *all-off* condition. If any are on, a 00 error halt results.
07	Load results memory	Load results memory with all 00 or all FF. Used as a delimiter for Function 53.
08	Record loop count	Record results memory loop count (150 loops).
09	Record interrupt step	Indicate to user which step has failed. Activated by time-out interrupt.
12	Record RS-232 lead status	Record RS-232 leads for display on CRT.
16	Wait for equal character	Wait for Q character to perform CRC check.
17	Wait for not-equal character	Wait for not-equal synchronization character to start receive-CRC calculation.
20	Trap character	Trap character received from delay line.
21	Trap first character in sequence	Same.
22	Trap characters within sequence	Same.
23	Trap last character in sequence	Same.
24	Increment results memory	Memory set.
25	Record until trap	Record until character from delay line is trapped.
26	Record next not-equal character	Record not-equal character received from delay line.
27	Load address register.	
28	Address register return.	
30	Record next character.	
33	Record character before trap.	
35	Record latch.	Loop unit back on itself (Mon sigs out ON). Record all transmitted data. Record all received data.
36	Record current character.	
37	Force into synchronization.	
38	Start CRC-16 calculation.	
39	Test CRC.	
40	Unconditional jump	Jump to all subroutines.
41	Preset jump.	

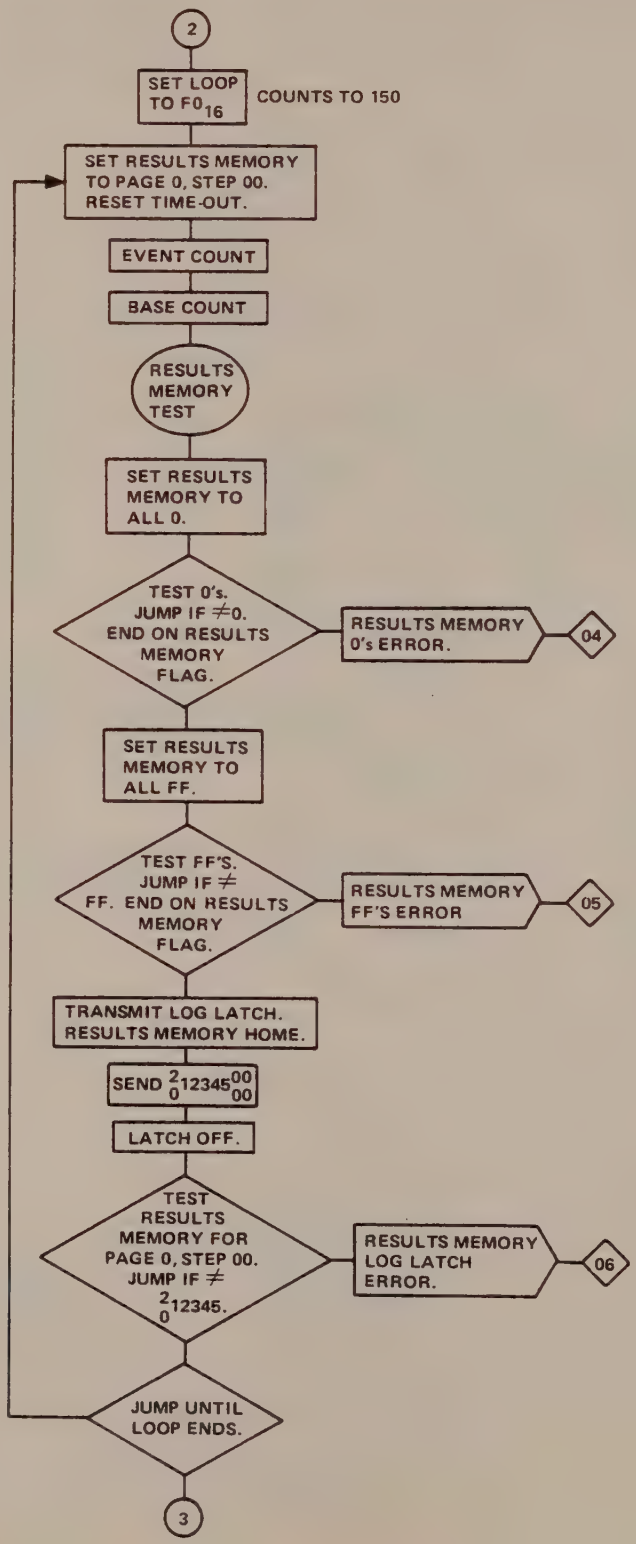
Table 4.1

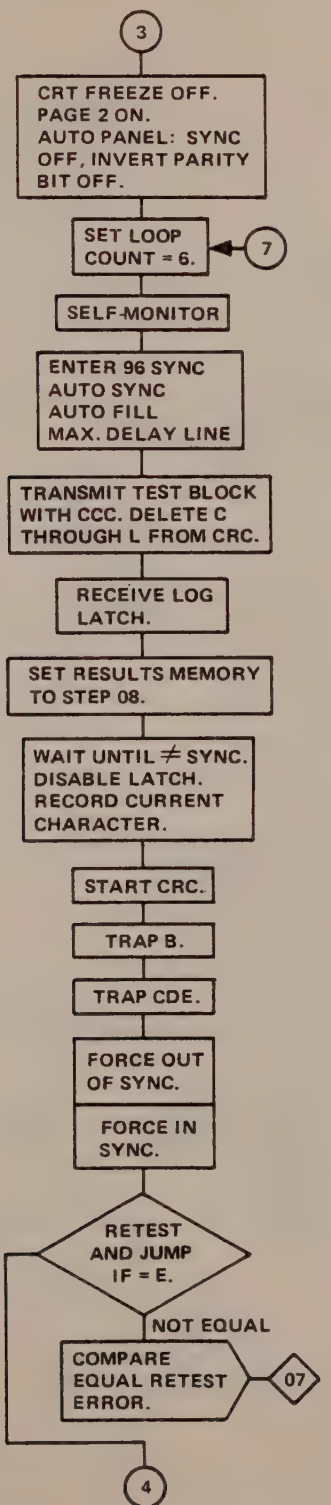
CRT Display	*Program Step*	*Halt or Function*	*Cause*
FF Failed	OC	0000	Bit switches are other than 00.
ET Failed	84	9617	Unable to detect sync. Defective delay line or transmitted data.
D2 Failed	12	0200	Flat 0 = 1 should be off.
ASCII fox messages displayed with END-TEST	—	0099	Only Page 2 displayed, not Page 1. Correct display ends with Pages 1 and 2 displayed; manually controllable.
9 Failed	39	0400	Results memory not all 00.
: Failed	3A	0500	Results memory not all FF.
J Failed	4A	0600	Log latch or parity failure.
BS Failed	88	4220	Trap failed or was not satisfied.
LF Failed	8A	C321	Trap sequence failed.
D4 Failed	94	0800	Failure of Jump if equal.
X Failed	F8	1300	—
EB Failed	97	C925	Trap failed.
(Failed	A8	0272	Detect in for on failed (no RTS)
- Failed	AD	0273	Detect in for off failed.
+ Failed	AB	0C00	Failure of Jump if DTR on.
" Failed	A7	0900	Failure of Jump if data greater than CTR.

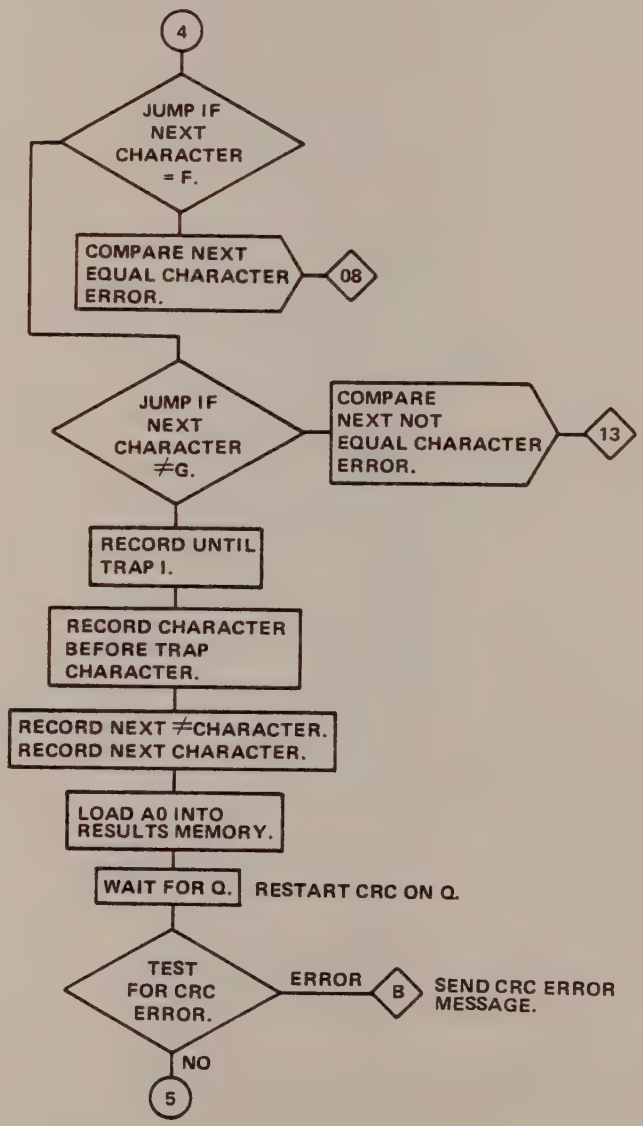
No.	*Description*	*Self-Test Use*
42	Set loop count	Test results memory 150 times. Loop back test, 6 times.
43	End loop.	
44	Jump if equal character.	
45	Jump if not-equal character.	
46	Retest and jump if equal character.	
47	Test flag	Test Flag 1 for ON condition upon restart Test Flag 0 for OFF upon installation. Test memory overflow flag until ON. Test memory overflow flag for ON.
48	Set results memory step	As intended.
49	Set results memory page	As intended.
50	Send character.	
52	Send results memory location.	
53	Send results memory until trap character	Send results memory trapped and recorded data to INTERVIEW for visual test.
54	Send results memory until trap function.	
55	Stop and Start CCC	Start and stop calculator, deleting character D from loopback test.
56	Invert parity bit	Latch on and off.
57	Load fill character.	
58	Start CRC-16 calculation.	
59	Send CRC.	
60	Send ASCII Fox message.	
63	Send EBCDIC message.	
65	Send EBCD message.	
66	Send Selectric message.	
70	Turn on RS-232 lead(s)	Visually check all leads, using LEDs.
71	Turn off RS-232 lead(s).	Turn off all leads at end of test.
72	Wait until test point is on	Test ON condition of RTS with INTERSHAKE in toward-modem mode (auto-panel modem).
73	Wait until test point is off	Test OFF condition of RTS with INTERSHAKE in toward-terminal mode (auto-panel terminal).
74	Interrupt if lead is on	Interrupt after RTS is on.
75	Interrupt if lead is off	Interrupt after RTS is off (interrupt lead tested).
76	Cancel Interrupt.	
77	Jump if lead is on	Test lead.
78	Jump if lead is off	Test lead.
80	Time delay	Time Clear CRT ON.
81	Time delay	Time Clear CRT ON.
82	Time delay	Time audible alarm ON, 0.5 sec.
84	Set time-out interrupt.	
85	Base Count.	
87	Counter control	Count loops in results memory test visually.
88	Jump if counter is greater than data	Test event counter for a value greater than 08. Should be 15.
89	Record loop count	Record 6 loopback counts.
90	Enter synchronization character	Loopback test (synchronization test).
91	Auto panel	Establish synchronous mode.
92	Auto panel speed	Set speed of test to 9600 bps.
93	Auto panel	Switch from modem to terminal testing. RS-232 housekeeping.
94	CRT controls	Test: Page 1, Page 2, Pages 1 and 2. Reverse video Half-intensity Blink Freeze Clear.
95	Auto synchronization	Force out of synchronization.
96	Delay line	Select 4 kbits for loopback test.
97	Interrupt	Time out.
98	Recycle test.	
99	END.	

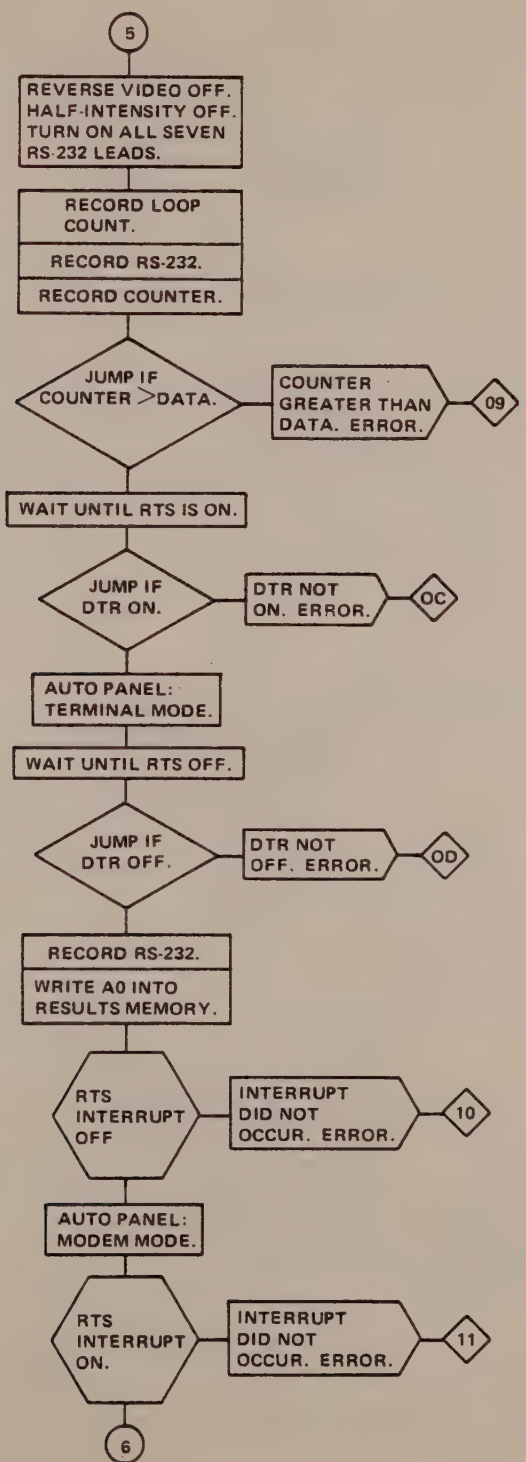
4.6 Program Flow Diagram

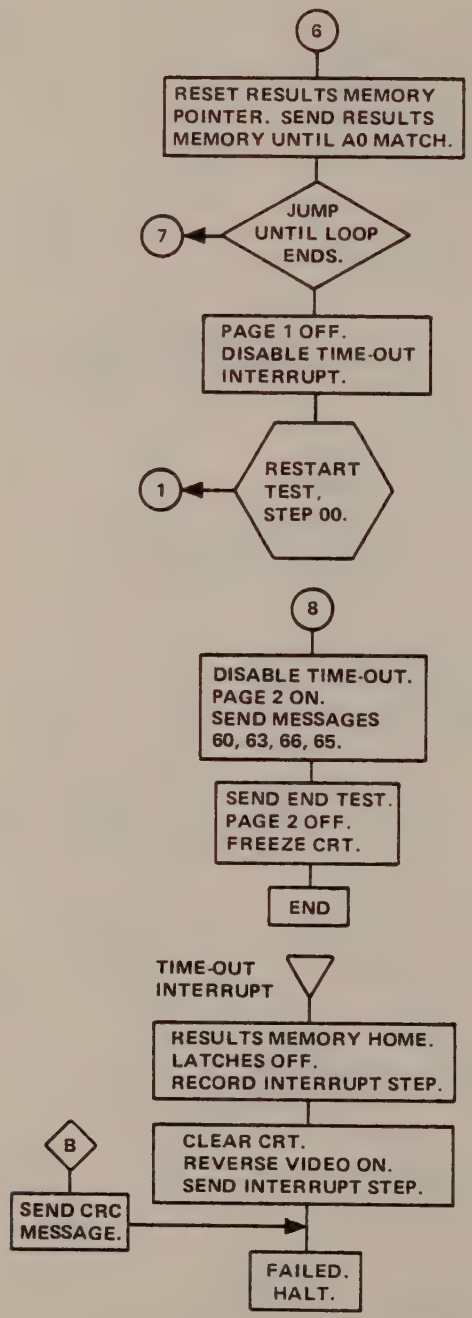



2
SET LOOP TO F0 16
COUNTS TO 150
SET RESULTS MEMORY TO PAGE 0, STEP 00. RESET TIME-OUT.
EVENT COUNT
BASE COUNT
RESULTS MEMORY TEST
SET RESULTS MEMORY TO ALL 0.
TEST 0's. JUMP IF ≠0. END ON RESULTS MEMORY FLAG.
RESULTS MEMORY 0's ERROR.
04
SET RESULTS MEMORY TO ALL FF.
TEST FF'S. JUMP IF ≠ FF. END ON RESULTS MEMORY FLAG.
RESULTS MEMORY FF'S ERROR
05
TRANSMIT LOG LATCH. RESULTS MEMORY HOME.
SEND 2 0 12345 00 00
LATCH OFF.
TEST RESULTS MEMORY FOR PAGE 0, STEP 00. JUMP IF ≠ 2 0 12345.
RESULTS MEMORY LOG LATCH ERROR.
06
JUMP UNTIL LOOP ENDS.
3


3
CRT FREEZE OFF.
PAGE 2 ON.
AUTO PANEL: SYNC
OFF, INVERT PARITY
BIT OFF.
SET LOOP
COUNT = 6.
7
SELF-MONITOR
ENTER 96 SYNC
AUTO SYNC
AUTO FILL
MAX. DELAY LINE
TRANSMIT TEST BLOCK
WITH CCC. DELETE C
THROUGH L FROM CRC.
RECEIVE LOG
LATCH.
SET RESULTS MEMORY
TO STEP 08.
WAIT UNTIL ≠ SYNC.
DISABLE LATCH.
RECORD CURRENT
CHARACTER.
START CRC.
TRAP B.
TRAP CDE.
FORCE OUT
OF SYNC.
FORCE IN
SYNC.
RETEST
AND JUMP
IF = E.
NOT EQUAL
COMPARE
EQUAL RETEST
ERROR.
07
4


4
JUMP IF NEXT CHARACTER = F.
COMPARE NEXT EQUAL CHARACTER ERROR.
08
JUMP IF NEXT CHARACTER ≠G.
COMPARE NEXT NOT EQUAL CHARACTER ERROR.
13
RECORD UNTIL TRAP I.
RECORD CHARACTER BEFORE TRAP CHARACTER.
RECORD NEXT ≠CHARACTER.
RECORD NEXT CHARACTER.
LOAD A0 INTO RESULTS MEMORY.
WAIT FOR Q.
RESTART CRC ON Q.
TEST FOR CRC ERROR.
ERROR
B
SEND CRC ERROR MESSAGE.
NO
5


5
REVERSE VIDEO OFF.
HALF-INTENSITY OFF.
TURN ON ALL SEVEN
RS-232 LEADS.
RECORD LOOP
COUNT.
RECORD RS-232.
RECORD COUNTER.
JUMP IF
COUNTER >DATA.
COUNTER
GREATER THAN
DATA. ERROR.
09
WAIT UNTIL RTS IS ON.
JUMP IF
DTR ON.
DTR NOT
ON. ERROR.
0C
AUTO PANEL:
TERMINAL MODE.
WAIT UNTIL RTS OFF.
JUMP IF
DTR OFF.
DTR NOT
OFF. ERROR.
0D
RECORD RS-232.
WRITE A0 INTO
RESULTS MEMORY.
RTS
INTERRUPT
OFF
INTERRUPT
DID NOT
OCCUR. ERROR.
10
AUTO PANEL:
MODEM MODE.
RTS
INTERRUPT
ON.
INTERRUPT
DID NOT
OCCUR. ERROR.
11
6


6
RESET RESULTS MEMORY POINTER. SEND RESULTS MEMORY UNTIL A0 MATCH.
7
JUMP UNTIL LOOP ENDS.
PAGE 1 OFF. DISABLE TIME-OUT INTERRUPT.
1
RESTART TEST, STEP 00.
8
DISABLE TIME-OUT. PAGE 2 ON. SEND MESSAGES 60, 63, 66, 65.
SEND END TEST. PAGE 2 OFF. FREEZE CRT.
END
TIME-OUT INTERRUPT
RESULTS MEMORY HOME. LATCHES OFF. RECORD INTERRUPT STEP.
B
CLEAR CRT. REVERSE VIDEO ON. SEND INTERRUPT STEP.
SEND CRC MESSAGE.
FAILED. HALT.

4.7 Program

INTERSHAKE II PROGRAM

TITLE: INTERSHAKE SELF TEST

FILE NO. 004A
SHEET 1 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 1 (0)		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 4 (0)	0	0	02	98	Test No-op function.	
	1	1	01	70	Test alarm (alarm on).	
	2	2	05	82	0.5-Second delay Function 82 test.	
	3	3	FF	71	Turn off alarm (turn off all leads).	
	4	4	06	27	Load address register: test Function 27.	
	5	5	EC	40	Go-to.	
	6	6	08	97	Disable interrupt selection group	
	7	7	FF	84	Set maximum delay time-out.	
	8	8	0C	97	Interrupt on time-out.	
	9	9	02	98	No-op.	
	A	10	0D	41	Load address register. Jump if bit switches off.	
	B	11	00	06	Test for all bit switches off.	
	C	12	00	00	Halt 00. Bit switch error.	
	D	13	C2	41	Load address register.	
	E	14	13	47	Jump if Flag 1 = 1 (Flag is off at start).	
	F	15	12	41	Load address register.	
D 9 5 (1)	0	16	02	47	Jump if Flag 0 = 0 (Flag is off at start).	
	1	17	02	00	Flag 0 error--should have been off.	
	2	18	11	47	Set Flag 1 = 1.	
	3	19	14	91	Auto panel.	
	4	20	01	56	Invert parity bit.	
	5	21	F0	92	Auto panel: 9.6 kbps.	
	6	22	11	94	Select INTERVIEW page 1.	
	7	23	51	94	Turn on reverse video.	
	8	24	D2	50	Send R. } Send	
	9	25	55	50	Send U. } RUNNING	
	A	26	4E	50	Send N. } to	
	B	27	CE	50	Send N: } INTERVIEW.	
	C	28	C9	50	Send I. }	
	D	29	4E	50	Send N. }	
	E	30	47	50	Send G. }	
	F	31	50	94	Turn off reverse video.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE: ASCII
SPEED: 9.6, 56 kbps
(ASYNC / SYNC)
SYN CHARACTER: 96
STOP BIT: 1.0 , 1.5 , 2.0
INFO BITS: ~~5 6 7~~ (8)
PARITY: (NONE , ODD , EVEN)
(CONTROL EIA / OFF)
ON-LINE: ~~TD/RD , TS , RD~~
OFF-LINE: (TERM / MODEM)
(MON SIGS) NORMAL
PATCH CORDS: Detect in to KTS 24 to 17 Mon to Sigs out
CONTROL EIA (V.24): ALL 7X positions.
COUNTER ZONE: Events (8X)
INTERRUPTS: RS-232
FLAGS: 0,1
LATCH: 0035

CONTINUE ON OTHER SIDE

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ALEXANDRIA, VA. 22314

CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A 6 2	0	32	31	94	Freeze CRT.	
	1	33	F0	42	Set loop count to 150.	
	2	34	00	49	Set results memory home.	
	3	35	03	87	Add to event count (test counter).	
	4	36	00	85	Add one to base count.	
	5	37	00	07	Load fill character 00 (All 0 bits).	
	6	38	25	41	Load address register.	
	7	39	82	47	Load RM with 00 till overflow flag on.	
	8	40	00	49	Set RM home (resets overflow flag).	
	9	41	39	41	Load address register.	
	A	42	00	29	Jump if RM position not = 00.	
	B	43	00	24	Increment RM address pointer one step.	
	C	44	29	41	Load address pointer.	
	D	45	82	47	Test for 00 in RM until overflow.	
	E	46	00	49	Set RM home (Resets overflow flag).	
	F	47	FF	07	Load fill character FF (all one bits).	
F B 7 3	0	48	2F	41	Load address register.	
	1	49	82	47	Load RM with FF till overflow flag on.	
	2	50	00	49	Set RM home (resets overflow flag).	
	3	51	3A	41	Load address register.	
	4	52	FF	29	Jump if RM position not = FF.	
	5	53	00	24	Increment RM address pointer one step.	
	6	54	3B	41	Load address register.	
	7	55	83	47	Jump when overflow flag = 1 = on.	
	8	56	33	40	Go-to.	
	9	57	04	00	Halt 4. Results memory not 00. Error.	
	A	58	05	00	Halt 5. Results memory not FF. Error.	
	B	59	31	94	Freeze CRT.	
	C	60	03	35	Latch record all transmit data.	
	D	61	00	49	Reset results memory home.	
	E	62	20	50	Send space to RM (record).	
	F	63	B0	50	Send 0 to RM (record).	

FILE NO. D04A
SHEET 1 B OF 4
PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 2 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL E-F
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 (4) 0	0	0	31	50	Send 1 to RM (record).	
	1	1	32	50	Send 2 to RM (record).	
	2	2	B3	50	Send 3 to RM (record).	
	3	3	34	50	Send 4 to RM (record).	
	4	4	B5	50	Send 5 to RM (record).	
	5	5	20	50	Send space to RM (not recorded).	
	6	6	00	35	Record transmit latch OFF.	
	7	7	00	49	Set results memory home.	
	8	8	4A	41	Load address register.	
	9	9	4B	40	Go-to. Jump around error halt if no error.	
	A	10	06	00	Halt 6. Log latch error.	
	B	11	20	29	Jump if space character not at RM home.	
	C	12	00	24	Increment RM address pointer.	
	D	13	B0	29	Jump if Ø not at RM +1.	
	E	14	00	24	Increment RM address pointer.	
	F	15	31	29	Jump if 1 not at RM +2.	
D 9 (5) 1	0	16	00	24	Increment RM address pointer.	
	1	17	32	29	Jump if 2 not at RM +3.	
	2	18	00	24	Increment RM address pointer.	
	3	19	B3	29	Jump if 3 not at RM +4.	
	4	20	00	24	Increment RM address pointer.	
	5	21	34	29	Jump if 4 not at RM +5.	
	6	22	00	24	Increment RM address pointer.	
	7	23	B5	29	Jump if 5 not at RM +6.	
	8	24	22	41	Load address register.	
	9	25	00	43	End loop count.	
	A	26	00	56	Set parity bit normal.	
	B	27	54	91	Auto panel.	
	C	28	30	94	CRT freeze off.	
	D	29	21	94	Select INTERVIEW page 2.	
	E	30	00	92	Set speed to 56 kbps.	
	F	31	06	42	Set loop count to 6.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE

SPEED

ASYNC / SYNC

SYN CHARACTER

STOP BIT
1.0 , 1.5 , 2.0

INFO BITS
5 , 6 , 7 , 8

PARITY
NONE , ODD , EVEN

CONTROL EIA / OFF

ON-LINE
TD/RD , TD , RD

OFF-LINE
TERM / MODEM

MON SIGS / NORMAL

PATCH CORDS

CONTROL EIA (V.24)

COUNTER ZONE

INTERRUPTS

FLAGS

LATCH

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 (1) 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A (6) 2	0	32	06	96	Enable delay line.	
	1	33	00	49	Set results memory home.	
	2	34	F7	93	Auto panel.	
	3	35	96	90	Load sync character, even-parity ASCII.	
	4	36	61	94	Turn on half-intensity video.	
	5	37	02	35	Self-monitor.	
	6	38	96	50	Send sync character.	
	7	39	96	50	Send sync character.	
	8	40	96	50	Send sync character.	
	9	41	41	50	Send A.	
	A	42	00	58	Start CRC-16 calculation.	
	B	43	50	54	Send space with Function 54.	
	C	44	42	50	Send B.	
	D	45	10	55	Stop calculator.	
	E	46	C3	50	Send C.	
	F	47	44	50	Send D.	
F B (7) 3	0	48	C5	50	Send E.	
	1	49	C6	50	Send F.	
	2	50	47	50	Send G.	
	3	51	48	50	Send H.	
	4	52	C9	50	Send I.	
	5	53	CA	50	Send J.	
	6	54	4B	50	Send K.	
	7	55	50	91	Auto panel.	
	8	56	CC	50	Send L.	
	9	57	54	91	Auto panel.	
	A	58	D1	50	Send Q.	
	B	59	00	55	Restart CCC calculator.	
	C	60	00	59	Send CCC.	
	D	61	00	15	Wait till Send complete.	
	E	62	00	35	Turn self-monitor latch off.	
	F	63	51	94	Turn on reverse video.	

FILE NO. D04A
SHEET 2B OF 4
PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM

ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 3 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 4 0	0	0	01	35	Record receive data latch on (records A).	
	1	1	00	49	Set results memory home.	
	2	2	06	48	Set RM address pointer to position 6.	
	3	3	F0	92	Set speed back to 9.6 kbps.	
	4	4	96	17	Wait until char ≠ Sync (A from delay line).	
	5	5	00	35	Latch off (0135 records A from delay line).	
	6	6	00	36	Record current character (still A).	
	7	7	00	38	Start receive CRC-16 calculation.	
	8	8	42	20	Trap character B.	
	9	9	10	55	Stop CCC calculator.	
	A	10	C3	21	Trap first character C.	
	B	11	44	22	Trap middle character D.	
	C	12	C5	23	Trap last character E.	
	D	13	16	95	Force out of synchronization.	
	E	14	00	37	Force back in synchronization.	
	F	15	92	41	Load address register.	
D 9 5 1	0	16	C5	46	Retest and jump = E.	
	1	17	07	00	Halt 7. Not E error.	
	2	18	95	41	Load address register.	
	3	19	C6	44	Jump if next character = F.	
	4	20	08	00	Halt 8. Next character was not F.	
	5	21	F9	41	Load address register.	
	6	22	47	45	Jump if char not equal to G.	
	7	23	C9	25	Record until Trap character I (HI).	
	8	24	CA	33	Record character before Trap J (I).	
	9	25	41	26	Record next not equal character (K).	
	A	26	00	30	Record next character (L).	
	B	27	D1	16	Wait for Q.	
	C	28	00	55	Restart CCC calculator.	
	D	29	F3	41	Load address register.	
	E	30	00	39	Test CCC. Jump if error.	
	F	31	50	94	Turn off reverse video.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE

SPEED

ASYNC / SYNC

SYN CHARACTER

STOP BIT 1.0 , 1.5 , 2.0

INFO BITS 5 , 6 , 7 , 8

PARITY NONE , ODD , EVEN

CONTROL EIA / OFF

ON-LINE TD/RD , TD , RD

OFF-LINE TERM / MODEM

MON SIGS / NORMAL

PATCH CORDS

CONTROL EIA (V.24)

COUNTER ZONE

INTERRUPTS

FLAGS

LATCH

CONTINUE ON OTHER SIDE

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CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 (2) 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E (A) 6 2	0	32	60	94	Turn off half-intensity video.	
	1	33	FE	70	Turn on all leads except alarm.	
	2	34	00	08	Record loop count.	
	3	35	00	12	Record RS-232 lead status.	
	4	36	00	89	Record counter.	
	5	37	A8	41	Load address register.	
	6	38	08	88	Jump if counter is greater than data (150).	
	7	39	09	00	Halt 9. Counter was not greater. Error.	
	8	40	02	72	Wait for RTS ON (should be on).	
	9	41	AC	41	Load address register.	
	A	42	08	77	Jump if DTR on (should be on).	
	B	43	0C	00	Halt 0C. DTR off. Error.	
	C	44	EF	93	Auto panel: terminal mode.	
	D	45	02	73	Wait until RTS off (should be off in terminal mode).	
	E	46	B1	41	Load address register.	
	F	47	08	78	Jump if DTR is off (should be off).	
F (B) 7 3	0	48	0D	00	Halt 0D. DTR error.	
	1	49	00	12	Record status in terminal mode.	
	2	50	A0	07	Load fill character used for Function 53.	
	3	51	80	75	Interrupt if RTS lead is off (should be off).	
	4	52	10	00	Halt 10. RTS error.	
	5	53	00	76	Disable lead interrupt.	
	6	54	F5	93	Auto panel: modem mode.	
	7	55	80	74	Interrupt if RTS is on (modem mode turned on RTS).	
	8	56	11	00	RTS error.	
	9	57	00	76	Disable lead interrupt.	
	A	58	00	49	Set results memory home.	
	B	59	00	52	Send first character for RM home position.	
	C	60	A0	53	Send RM through A0 (space).	
	D	61	61	41	Load address register.	
	E	62	00	43	End loop (count 6).	
	F	63	10	94	Select INTERVIEW page 1.	

FILE NO. D04A
SHEET 3B OF 4
PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: DATE

COMPANY NAME: TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

INTERSHAKE II PROGRAM

TITLE:

FILE NO. D04A
SHEET 4 OF 4

DESCRIPTION:

PROGRAM LOCATION
DTM S/N
CELL E - F
RAM
PROM

OBJECTIVE:

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNC-TION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
C 8 4 0	0	0	08	97	Disable time-out interrupt.	
	1	1	00	98	Recycle test.	
	2	2	08	97	Disable time-out interrupt.	
	3	3	C5	27	Load address register.	
	4	4	EC	40	Go-to.	
	5	5	01	60	Send ASCII fox message from G PROM.	
	6	6	99	83	Wait 99 bit times.	
	7	7	01	63	Send EBCDIC message.	
	8	8	01	66	Send Selectric message.	
	9	9	01	65	Send EBCD message.	
	A	10	71	94	Turn on blinking video.	
	B	11	51	94	Turn on reverse video.	
	C	12	C5	50	Send E.	
	D	13	4E	50	Send N.	
	E	14	44	50	Send D	Send END-TEST message
	F	15	2D	50	Send −.	
D 9 5 1	0	16	D4	50	Send T.	
	1	17	C5	50	Send E.	
	2	18	53	50	Send S.	
	3	19	D4	50	Send T.	
	4	20	20	94	Turn off INTERVIEW page 2.	
	5	21	31	94	Freeze CRT.	
	6	22	02	98	No-op.	
	7	23	00	99	END. Complete light on.	
	8	24	00	49	Set results memory home.	
	9	25	F0	92	Set speed to 9.6 kbps.	
	A	26	00	35	Turn off log latch modes.	
	B	27	00	09	Record interrupted step.	
	C	28	F0	92	Set speed to 9.6 kbps.	
	D	29	E0	27	Load address register.	
	E	30	30	94	Unfreeze CRT.	
	F	31	EC	40	Go-to.	

APPLICABLE INFORMATION (WRITE IN OR CIRCLE)

CODE
SPEED
ASYNC / SYNC
SYN CHARACTER
STOP BIT 1.0 , 1.5 , 2.0
INFO BITS 5 , 6 , 7 , 8
PARITY NONE , ODD , EVEN
CONTROL EIA / OFF
ON-LINE TD/RD , TD , RD
OFF-LINE TERM / MODEM
MON SIGS / NORMAL
PATCH CORDS
CONTROL EIA (V.24)
COUNTER ZONE
INTERRUPTS
FLAGS
LATCH

CONTINUE ON OTHER SIDE

ATLANTIC RESEARCH CORP.
ALEXANDRIA, VA. 22314

CONTINUE ON OTHER SIDE

ADDRESS PAGE (CIRCLE ONE) 3 2 1 0		ENTRY STEP	DATA	FUNCTION	FUNCTION DESCRIPTION/COMMENTS	JUMP ← →
E A 6 2	0	32	00	49	Set results memory home.	
	1	33	51	94	Turn off reverse video.	
	2	34	00	52	Send recorded interrupt step to CRT.	
	3	35	A0	50	Send space.	
	4	36	C6	50	Send F.	
	5	37	41	50	Send A.	
	6	38	C9	50	Send I.	Send
	7	39	CC	50	Send L.	FAILED
	8	40	C5	50	Send E.	message
	9	41	44	50	Send D.	
	A	42	31	94	Freeze CRT.	
	B	43	12	00	Halt 12.	
	C	44	08	97	Disable time-out interrupt.	
	D	45	02	81	Delay.	
	E	46	01	94	CRT clear ON.	
	F	47	FF	57	Load fill character.	
F B 7 3	0	48	02	80	Delay.	
	1	49	00	94	CRT clear OFF.	
	2	50	00	28	Branch and link. Return.	
	3	51	E5	27	Load address register.	
	4	52	EC	40	Go-to.	
	5	53	C3	50	Send C.	Send CRC
	6	54	D2	50	Send R.	FAILED
	7	55	C3	50	Send C.	message.
	8	56	E3	40	Go-to.	
	9	57	13	00	Halt 13.	
	A	58	E1	E1	End of file.	
	B	59	B9	40	Go-to.	
	C	60	B5	40	Go-to.	
	D	61	08	97	Disable selection interrupt.	
	E	62	00	76	Disable interrupt lead.	
	F	63	D8	40	Go-to.	

FILE NO. D04A
SHEET 4 OF 4
PROGRAM LOCATION
DTM S/N
CELL E-F
RAM
PROM
ADDITIONAL INFORMATION (WRITE IN)

ADDITIONAL REMARKS

PROGRAM WRITTEN BY: John A. Mansker DATE

COMPANY NAME: Atlantic Research Corporation. TEL. NO.

ADDRESS:

FORM NO. TP-139-6-77

4.8 Inter-KEY Program Listing

```
Eg
0298 nop  3150 XMT  0135 REC  0897 INT
0170 232  3250 XMT  0049 -RM  0098 nop
0582 DLY  B350 XMT  0648 -RM  0897 INT
FF71 232  3450 XMT  F092 AUT  C527 PRE
0627 PRE  B550 XMT  9617 TRP  EC40 JMP
EC40 JMP  2050 XMT  0035 REC  0160 MSG
0897 INT  0035 REC  0036 REC  9983 DLY
FF84 INT  0049 -RM  0038 BCC  0163 MSG

0C97 INT  4A41 PRE  4220 TRP  0166 MSG
0298 nop  4B40 JMP  1055 xmt  0165 MSG
0D41 PRE  0600 HLT  C321 TRP  7194 AUX
0006 JSW  2029 JEM  4422 TRP  5194 AUX
0000 HLT  0024 -RM  C523 TRP  C550 XMT
C241 PRE  B029 JEM  1695 SYN  4E50 XMT
1347 JFG  0024 -RM  0037 SYN  4450 XMT
1241 PRE  3129 JEM  9241 PRE  2D50 XMT

0247 JFG  0024 -RM  C546 RTJ  D450 XMT
0200 HLT  3229 JEM  0700 HLT  C550 XMT
1147 FLG  0024 -RM  9541 PRE  5350 XMT
1491 AUT  B329 JEM  C644 JEC  D450 XMT
0156 xmt  0024 -RM  0800 HLT  2094 AUX
F092 AUT  3429 JEM  F941 PRE  3194 AUX
1194 AUX  0024 -RM  4745 JNC  0298 nop
5194 AUX  B529 JEM  C925 REC  0099 END

D250 XMT  2241 PRE  CA33 REC  0049 -RM
5550 XMT  0043 JEL  4126 REC  F092 AUT
4E50 XMT  0056 xmt  0030 REC  0035 REC
CE50 XMT  5491 AUT  B116 TRP  0009 RCD
C950 XMT  3094 AUX  0055 xmt  F092 AUT
4E50 XMT  2194 AUX  F341 PRE  E027 PRE
4750 XMT  0092 AUT  0039 JBE  3094 AUX
5094 AUX  0642 PRE  5094 AUX  EC40 JMP

3194 AUX  0696 AUT  6094 AUX  0049 -RM
F042 PRE  0049 -RM  FE70 232  5194 AUX
0049 -RM  F793 AUT  0008 RCD  0052 XMT
0387 CTR  9690 SYN  0012 REC  A050 XMT
0085 CTR  6194 AUX  0089 CTR  C650 XMT
0007 BSW  0235 REC  A841 PRE  4150 XMT
2541 PRE  9650 XMT  0888 JCT  C950 XMT
8247 JFG  9650 XMT  0900 HLT  CC50 XMT

0049 -RM  9650 XMT  0272 232  C550 XMT
3941 PRE  4150 XMT  AC41 PRE  4450 XMT
0029 JEM  0058 BCC  0877 JIO  3194 AUX
0024 -RM  5054 XMT  0C00 HLT  1200 HLT
2941 PRE  4250 XMT  EF93 AUT  0897 INT
8247 JFG  1055 xmt  0273 232  0281 DLY
0049 -RM  C350 XMT  B141 PRE  0194 AUX
FF07 BSW  4450 XMT  0878 JIO  FF57 xmt

2F41 PRE  C550 XMT  0D00 HLT  0280 DLY
8247 JFG  C650 XMT  0012 REC  0094 AUX
0049 -RM  4750 XMT  A007 BSW  0028 RET
3A41 PRE  4850 XMT  8025 INT  F522 PRE
FF29 JEM  C950 XMT  1000 HLT  EC40 JMP
0024 -RM  CA50 XMT  0076 INT  C350 XMT
3B41 PRE  4B50 XMT  F593 AUT  D250 XMT
8347 JFG  5091 AUT  8074 INT  C350 XMT

3340 JMP  CC50 XMT  1100 HLT  E340 JMP
0400 HLT  5491 AUT  0076 INT  1300 HLT
0500 HLT  D150 XMT  0049 -RM  E1E1 EOF
3194 AUX  0055 xmt  0052 XMT  B940 JMP
0335 REC  0059 BCC  A053 XMT  B540 JMP
0049 -RM  0015 DLY  6141 PRE  0897 INT
2050 XMT  0035 REC  0043 JEL  0076 INT
B050 XMT  5194 AUX  1094 AUX  D840 JMP
s_
```

Appendix A

Message Content, PROM 842G-001B

0D	0A	54 T	68 h	65 e	20 SP	51 Q	75 u	69 i	63 c	6B k	20 SP	42 B	72 r	6F o	77 w
6E n	20 SP	46 F	6F o	78 x	20 SP	4A J	75 u	6D m	70 p	73 s	20 SP	4F O	76 v	65 e	72 r
20 SP	54 T	68 h	65 e	20 SP	4C L	61 a	7A z	79 y	20 SP	44 D	6F o	67 g	27 '	73 s	20 SP
42 B	61 a	63 c	6B k	2E .	20 SP	20 SP	31 1	32 2	33 3	34 4	35 5	36 6	37 7	38 8	39 9
30 0	20 SP	20 SP	54 T	45 E	53 S	54 T	49 I	4E N	47 G						

FUNCTION 60: ASCII fox message, 72 characters

0D	0A	49 I	4E N	54 T	45 E	52 R	53 S	48 H	41 A	4B K	45 E	20 SP	41 A	6E n	61 a
6C l	79 y	7A z	65 e	73 s	20 SP	41 A	6E n	64 d	20 SP	46 F	69 i	6E n	64 d	73 s	20 SP
59 Y	6F o	75 u	72 r	20 SP	44 D	61 a	74 t	61 a	20 SP	43 C	6F o	6D m	6D m	75 u	6E n
69 i	63 c	61 a	74 t	69 i	6F o	6E n	73 s	20 SP	50 P	72 r	6F o	62 b	6C l	65 e	6D m
73 s	20 SP	46 F	61 a	73 s	74 t	21 !	20 SP	31 1	32 2	33 3	34 4	35 5	36 6	37 7	38 8
39 9	30 0														

FUNCTION 61: ASCII Test message, 80 characters.

0D	0A	49 I	4E N	54 T	45 E	52 R	53 S	48 H	41 A	4B K	45 E	20 SP	61 a	6E n	64 d
20 SP	49 I	4E N	54 T	45 E	52 R	56 V	49 I	45 E	57 W	20 SP	4A J	6F o	69 i	6E n	20 SP
54 T	6F o	67 g	65 e	74 t	68 h	65 e	72 r	20 SP	54 T	6F o	20 SP	51 Q	75 u	69 i	63 c
6B k	6C l	79 y	20 SP	53 S	69 i	6D m	75 u	6C l	61 a	74 t	65 e	20 SP	41 A	6E n	64 d
20 SP	41 A	6E n	61 a	6C l	79 y	7A z	65 e	20 SP	59 Y	6F o	75 u	72 r	20 SP	44 D	61 a
74 t	61 a	20 SP	43 C	6F o	6D m	6D m	75 u	6E n	69 i	63 c	61 a	74 t	69 i	6F o	6E n
73 s	20 SP	50 P	72 r	6F o	62 b	6C l	65 e	6D m	73 s	21 !	20 SP	31 1	32 2	33 3	34 4
35 5	36 6	37 7	38 8	39 9	30 0	20 SP	23 #	26 &	40 @	2F /	2D –				

FUNCTION 62: ASCII test message, 122 characters.

15	0D	25	C9 I	D5 N	E3 T	C5 E	D9 R	E2 S	C8 H	C1 A	D2 K	C5 E	40 SP	C1 A	95 n
81 a	93 l	A8 y	A9 z	85 e	A2 s	40 SP	C1 A	95 n	84 d	40 SP	C6 F	89 i	95 n	84 d	A2 s
40 SP	E8 Y	96 o	A4 u	99 r	40 SP	C4 D	81 a	A3 t	81 a	40 SP	C3 C	96 o	94 m	94 m	A4 u
95 n	89 i	83 c	81 a	A3 t	89 i	96 o	95 n	A2 s	40 SP	D7 P	99 r	96 o	82 b	93 l	85 e
94 m	A2 s	40 SP	C6 F	81 a	A2 s	A3 t	5A !	40 SP	F1 1	F2 2	F3 3	F4 4	F5 5	F6 6	F7 7
F8 8	F9 9	F0 0													

FUNCTION 63: EBCDIC test message, 80 characters.

15	0D	25	C9 I	D5 N	E3 T	C5 E	D9 R	E2 S	C8 H	C1 A	D2 K	C5 E	40 SP	81 a	95 n
84 d	40 SP	C9 I	D5 N	E3 T	C5 E	D9 R	E5 V	C9 I	C5 E	E6 W	40 SP	D1 J	96 o	89 i	95 n
40 SP	E3 T	96 o	87 g	85 e	A3 t	88 h	85 e	99 r	40 SP	E3 T	96 o	40 SP	D8 Q	A4 u	89 i
83 c	92 k	93 l	A8 y	40 SP	E2 S	89 i	94 m	A4 u	93 l	81 a	A3 t	85 e	40 SP	C1 A	95 n
84 d	40 SP	C1 A	95 n	81 a	93 l	A8 y	A9 z	85 e	40 SP	E8 Y	96 o	A4 u	99 r	40 SP	C4 D
81 a	A3 t	81 a	40 SP	C3 C	96 o	94 m	94 m	A4 u	95 n	89 i	83 c	81 a	A3 t	89 i	96 o
95 n	A2 s	40 SP	D7 P	99 r	96 o	82 b	93 l	85 e	94 m	A2 s	5A !	40 SP	F1 1	F2 2	F3 3
F4 4	F5 5	F6 6	F7 7	F8 8	F9 9	F0 0	40 SP	7B #	50 &	7C @	61 /	60 –			

FUNCTION 64: EBCDIC test message, 122 characters.

1C UC ( )	67 I	29 N	32 T	6B E	25 R	52 S	07 H	23 A	51 K	6B E	40 SP	23 A	29 N	0B D	40 SP
67 I	29 N	32 T	6B E	25 R	2A V	67 I	6B E	1A W	40 SP	61 J	19 O	67 I	29 N	40 SP	32 T
19 O	3B G	6B E	32 T	07 H	6B E	25 R	40 SP	32 T	19 O	40 SP	45 Q	4A U	67 I	73 C	51 K
31 L	46 Y	40 SP	52 S	67 I	49 M	4A U	31 L	23 A	32 T	6B E	40 SP	23 A	29 N	0B D	40 SP
23 A	29 N	23 A	31 L	46 Y	26 Z	6B E	40 SP	46 Y	19 O	4A U	25 R	40 SP	1F LC ( )	0B d	23 a
32 t	23 a	40 SP	73 c	19 o	49 m	49 m	4A u	29 n	67 i	73 c	23 a	32 t	67 i	19 o	29 n
52 s	40 SP	79 p	25 r	19 o	13 b	31 l	6B e	49 m	52 s	1C UC ( )	75 !	40 SP	1F LC ( )	20 1	10 2
30 3	08 4	68 5	58 6	38 7	04 8	64 9	54 0	40 SP	34 #	43 &	02 @	62 /	01 –	6D	

FUNCTION 65: EBCD test message, 122 characters.

1C UC ( )	19 I	52 N	02 T	4A E	29 R	25 S	26 H	79 A	1A K	4A E	40 SP	79 A	52 N	2A D	40 SP
19 I	52 N	02 T	4A E	29 R	31 V	19 I	4A E	75 W	40 SP	43 J	45 O	19 I	52 N	40 SP	02 T
45 O	23 G	4A E	02 T	26 H	4A E	29 R	40 SP	02 T	45 O	40 SP	5B Q	32 U	19 I	7A C	1A K
46 L	67 Y	40 SP	25 S	19 I	61 M	32 U	46 L	79 A	02 T	4A E	40 SP	79 A	52 N	2A D	40 SP
79 A	52 N	79 A	46 L	67 Y	54 Z	4A E	40 SP	67 Y	45 O	32 U	29 R	40 SP	1F LC ( )	2A d	79 a
02 t	79 a	40 SP	7A c	45 o	61 m	61 m	32 u	52 n	19 i	7A c	79 a	02 t	19 i	45 o	52 n
25 s	40 SP	0B p	29 r	45 o	76 b	46 l	4A e	61 m	25 s	01 !	40 SP	20 1	10 2	70 3	04 4
08 5	58 6	68 7	38 8	34 9	64 0	40 SP	1C UC ( )	70 #	68 &	10 @	1F LC ( )	07 /	37 –	6D	

FUNCTION 66: Selectric test message, 122 characters.

08	02	1F [LTRS]	10 T	14 H	01 E	04 SP	17 Q	07 U	06 I	0E C	0F K	04 SP	19 B	0A R	18 O
13 W	0C N	04 SP	0D F	18 O	1D X	04 SP	0B J	07 U	1C M	16 P	05 S	04 SP	18 O	1E V	01 E
0A R	04 SP	10 T	14 H	01 E	04 SP	12 L	03 A	11 Z	15 Y	04 SP	09 D	18 O	1A G	1B [FIGS]	0B '
1F [LTRS]	05 S	04 SP	19 B	03 A	0E C	0F K	1B [FIGS]	1C .	04 SP	04 SP	17 1	13 2	01 3	0A 4	10 5
15 6	07 7	06 8	18 9	16 0	04 SP	04 SP	1F [LTRS]	10 T	01 E	05 S	10 T	06 I	0C N	1A G	

FUNCTION 67: Baudot fox message, 72 characters.

Appendix B

INTERSHAKE Controls and Indicators